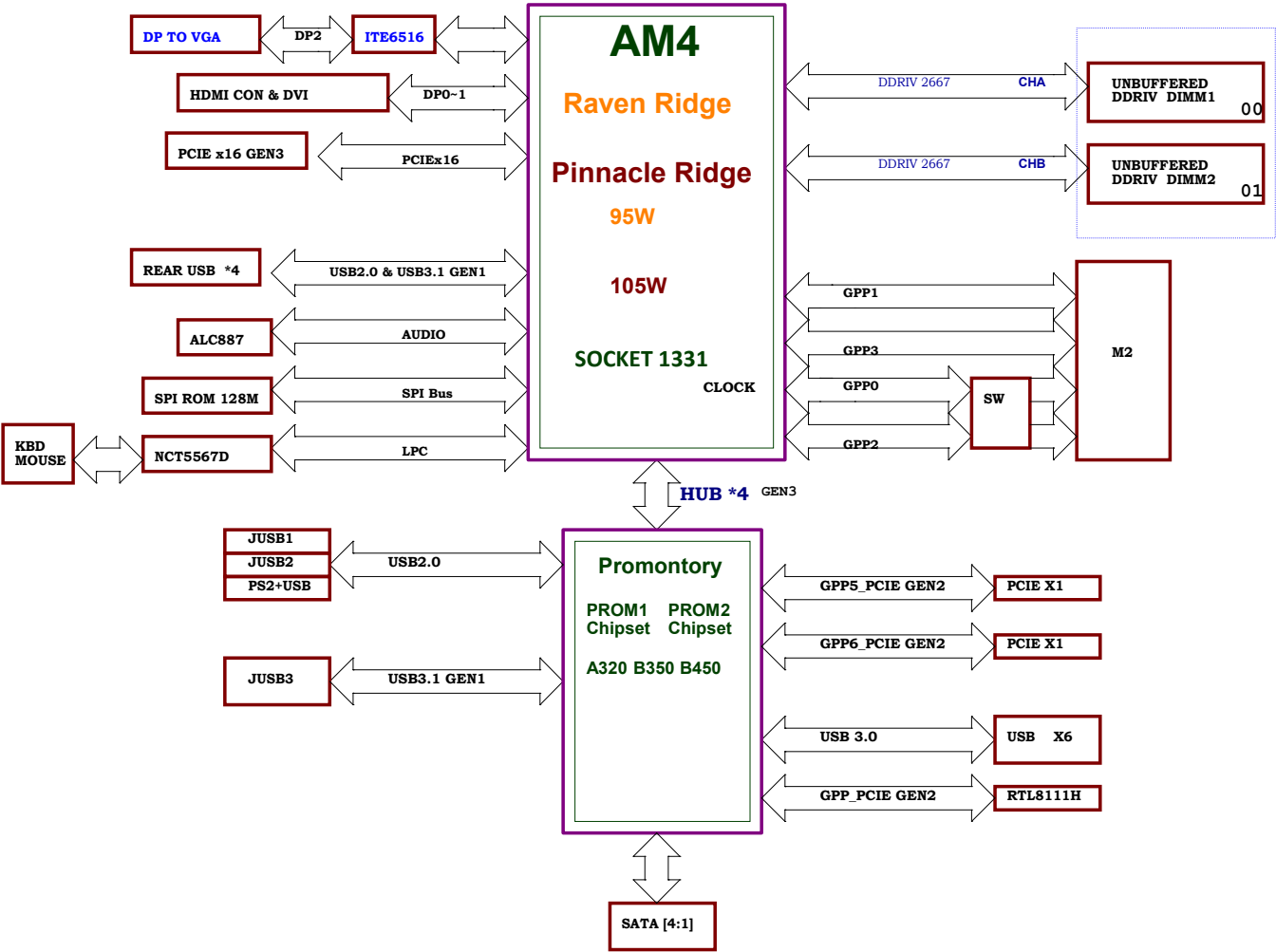


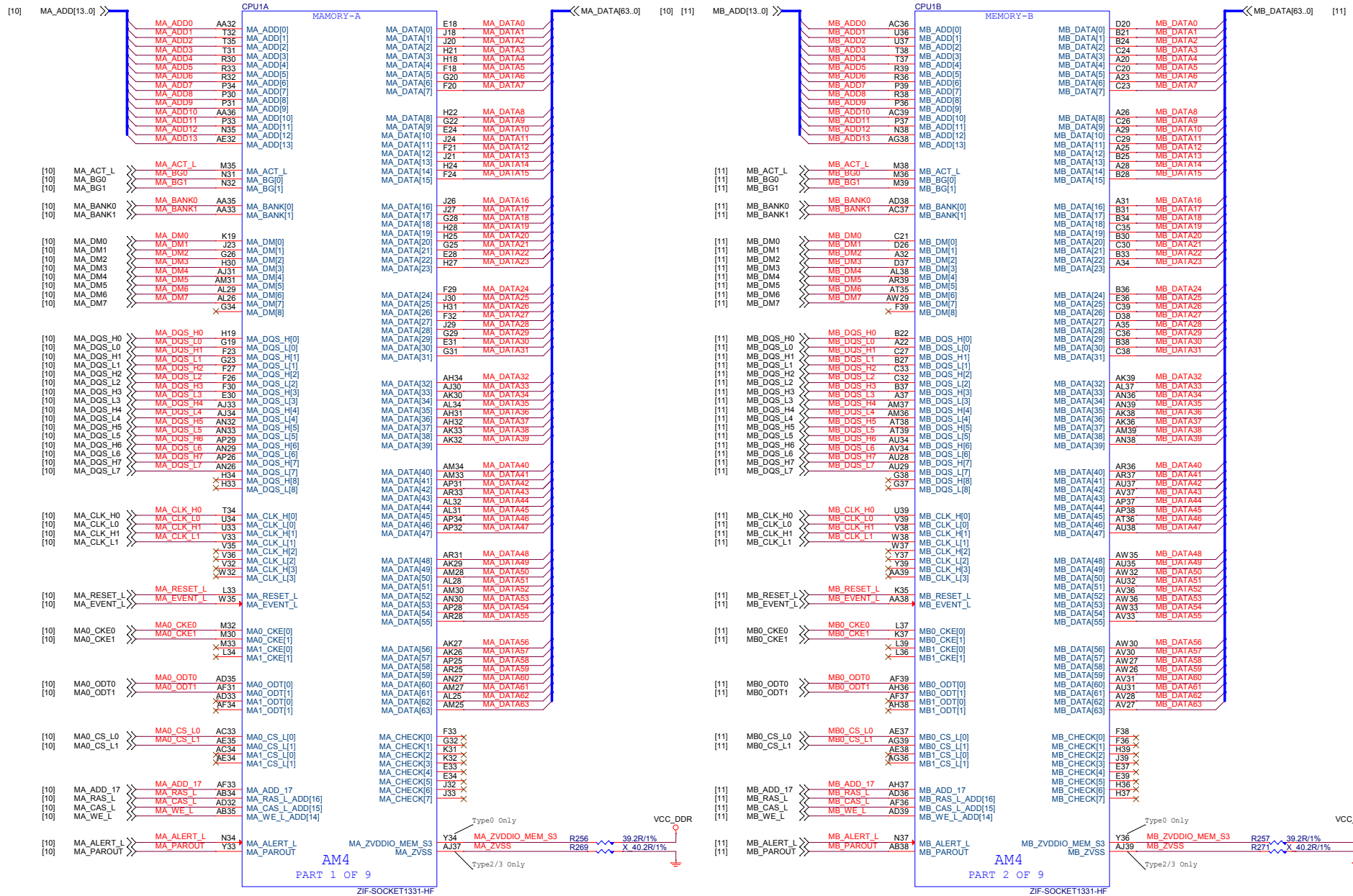
MS-7B84 Ver:20

- CPU:**
AMD AM4
- System Chipset:**
Promontory A320 & B450
(Value DIY or System Builder)
- Main Memory:**
DDR IV * 2 MAX:32 GB
- VRM**
UP9505 4+2
- On Board Chipset:**
LPC Super I/O --NCT5567
LAN RTL8111H
Azalia CODEC - Realtek ALC887
- Expansion Slots:**
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
M2_2 * 1
- OCF IC:**
RT9553B

FUSION BLOCK DIAGRAM



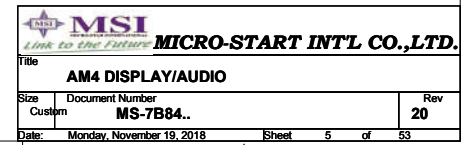
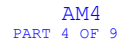
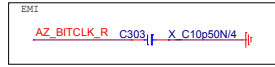
01 Block Diagram	37 CPU Power VDDP-MP8712
02 Cover Sheet	38 CPU Power Connector/PWRGD
03 FM4 DDR4 I/F	39 CPU Power RT8894 3+2 Phase
04 AM4 PCIE/SATAE	40/41 CPU Power Phase 1-4
05 AM4 Display/Audio	42 CPU Power NB Phase 1-2
06 AM4 SVI/ACPI/GPIO	43 CPU Power NB Switch/NCT3933
07 AM4 LPC/SPI/USB/CLK/STRAP	44 RT9553B CURRENT SENSE
08 AM4 Power/RTC Power/ 09 AM4 GND	45 ATX/Front Panel
10,11 DDR4-DIMM CH-A/B	46 ALL LED Control
12,13 DDR4-POWER/GND	47 BOM Option
14 Promontory-PCIE/SATA/SATAE	48 RTC Circuit/Moat Cap
15 Promontory-USB/OC	49 M2_2
16 Promontory-CLK/ACPI/GPIO	50 History
17 Promontory-Power / 18 Promontory-GND	51 Power Sequence
19 PCIE X16(X1*2) SLOT	52 Power Delivery
20 SIO NCT5567D	53 GPIO MAP
21 DVI Connector	
22 CPU/SYS FAN Control TYPE K	
23 / 24 / 25 LAN-RTL8111H/Audio ALC887	
26 USB Rear PS2+USB2.0	
27 USB Rear LAN+USB3.1 GEN1	
28 USB Front Side	
29 SATA Connector	
30 HDMI Connector	
31 DP to VGA RTD2166	
32 ACPI uPI-5VDIMM&3VSB	
33 PM-SY8288RAC-1.05V/GS7133-2.5V	
34 DDR PWR VPP25/VTT-MP2147	
35 DDR Power-RT8231AGQW	
36 CPU Power 1P8V-MP2147	



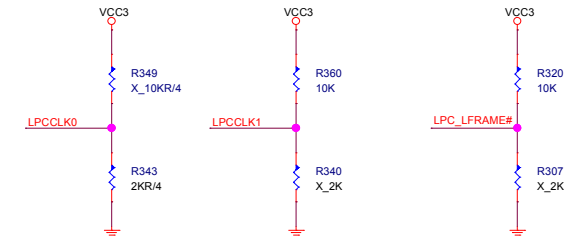
Schematic Cfg

Project

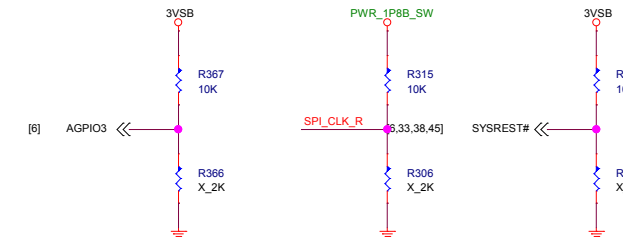
V A



Strapping Options

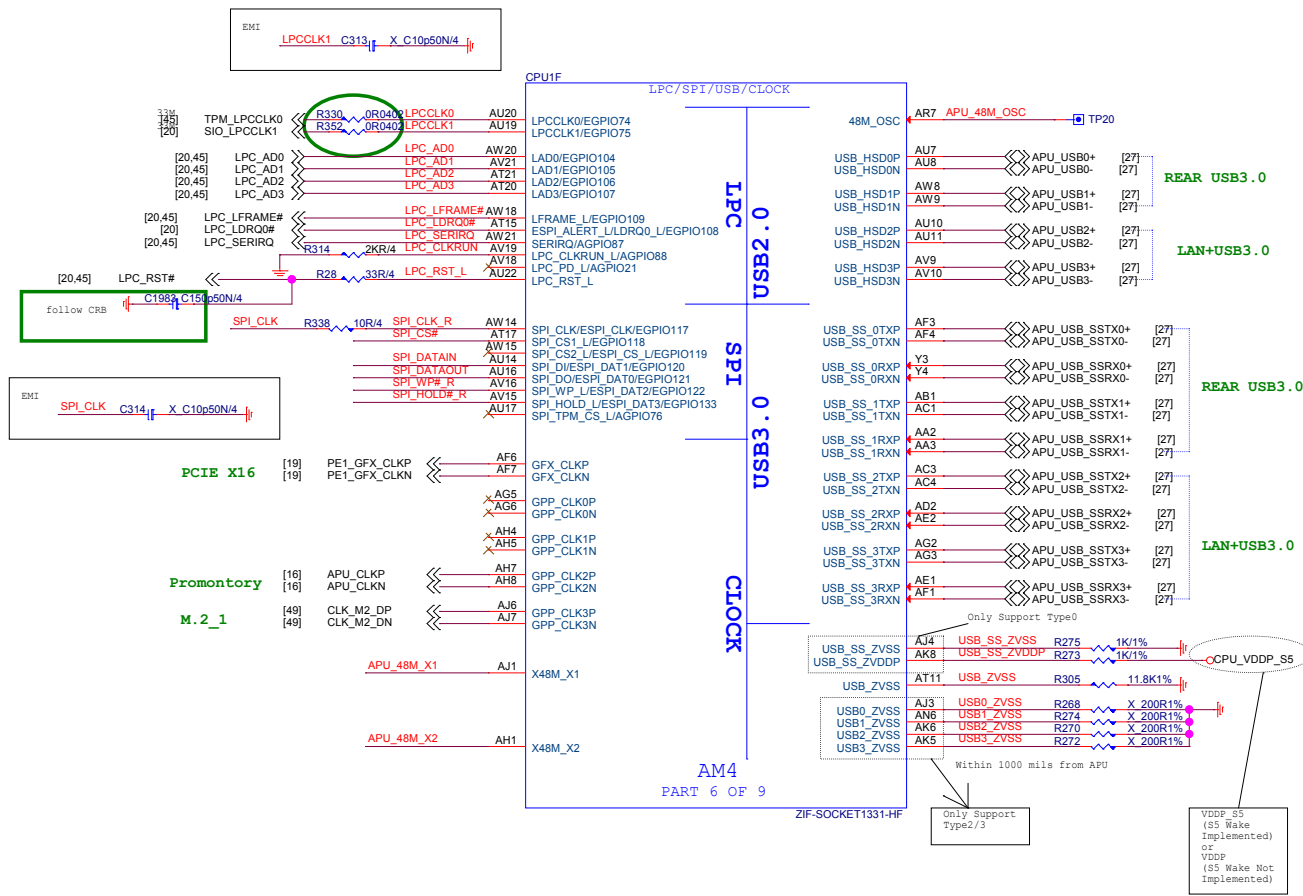


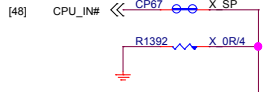
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ????	LPC ROM



	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

	RTCCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

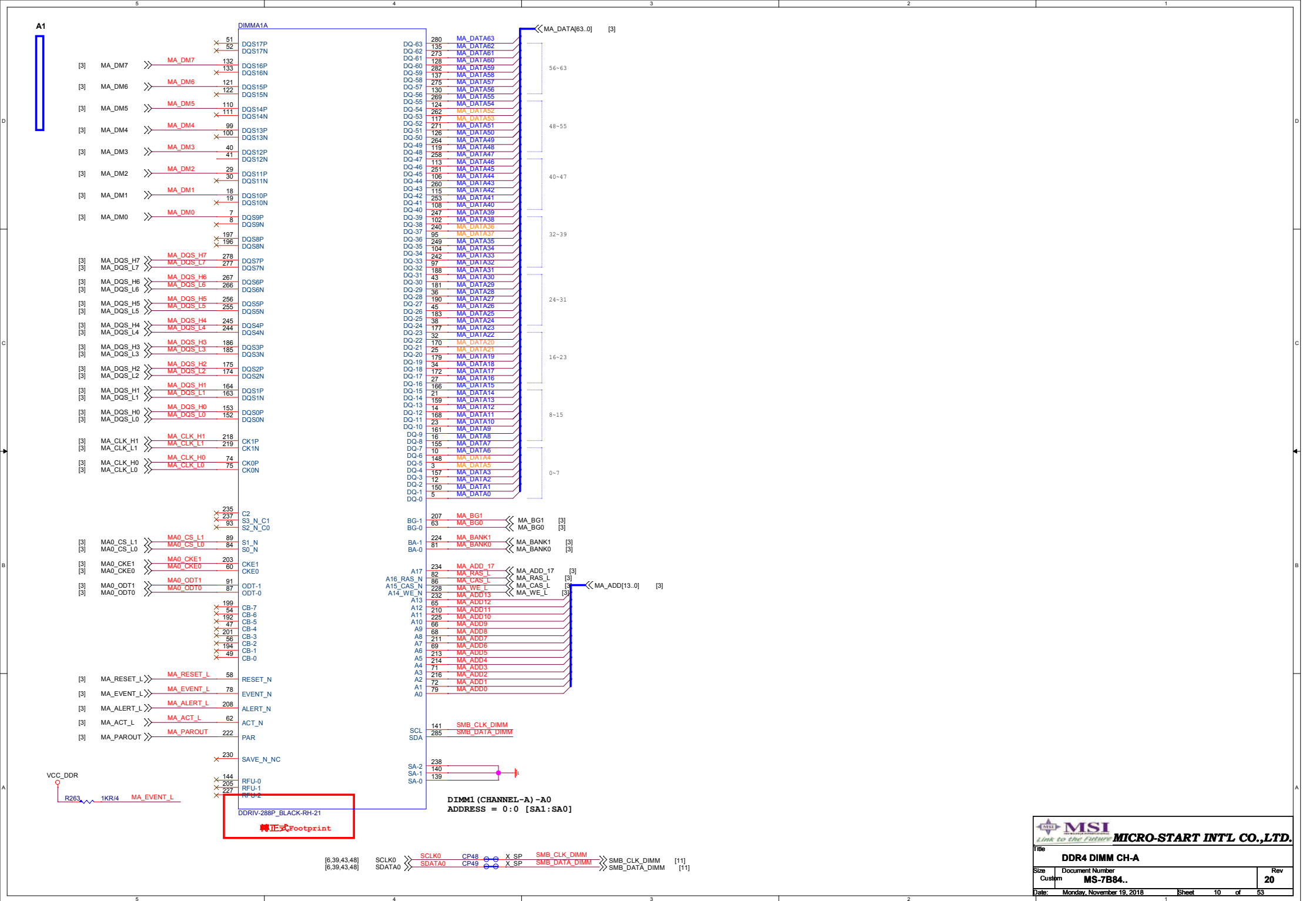


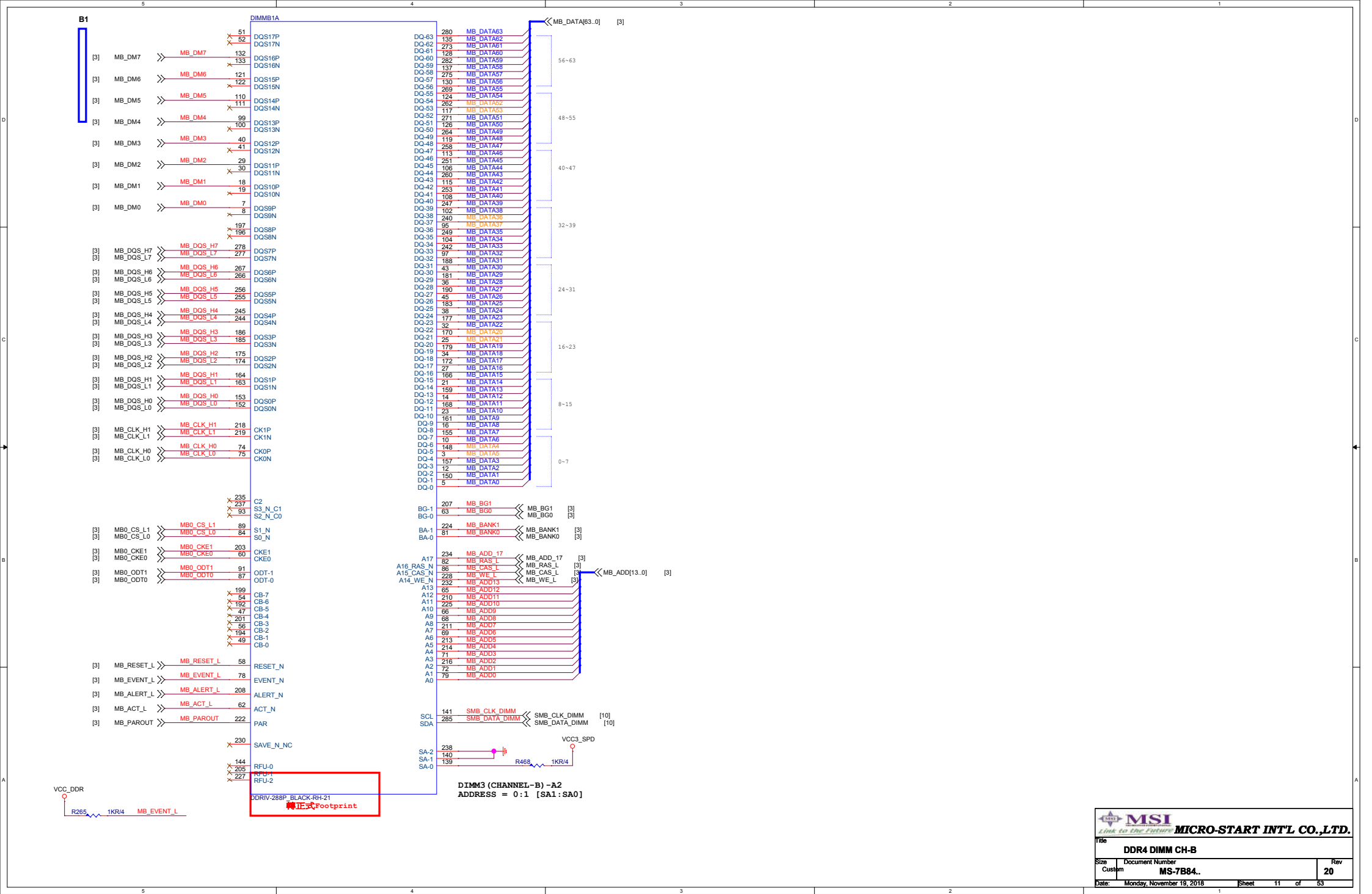


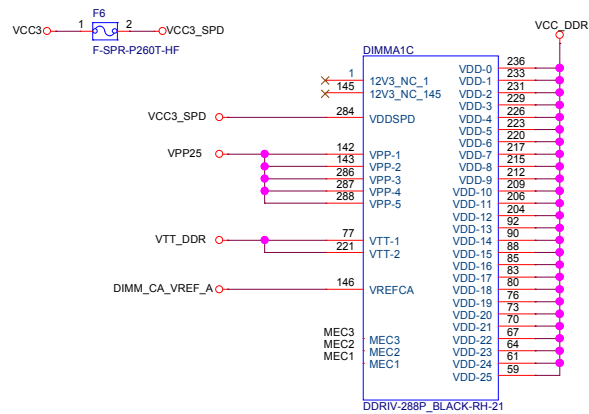
GND

AM4
PART 9 OF 9

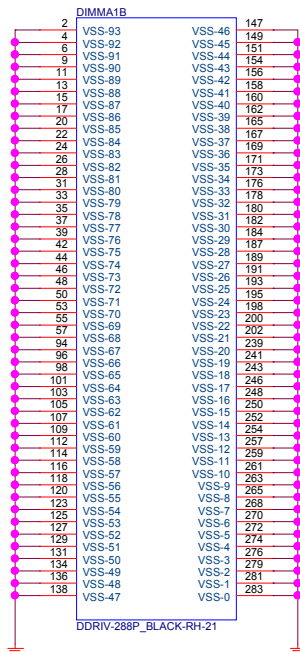
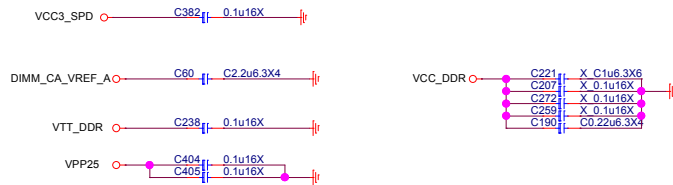






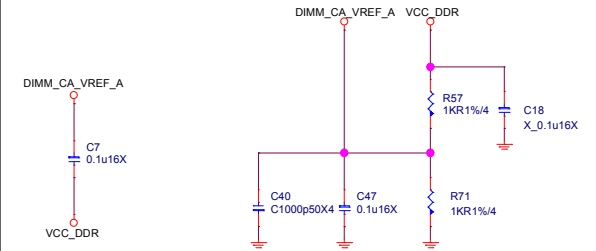


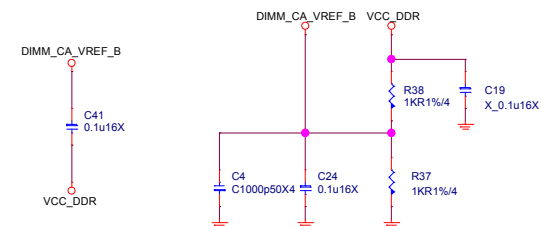
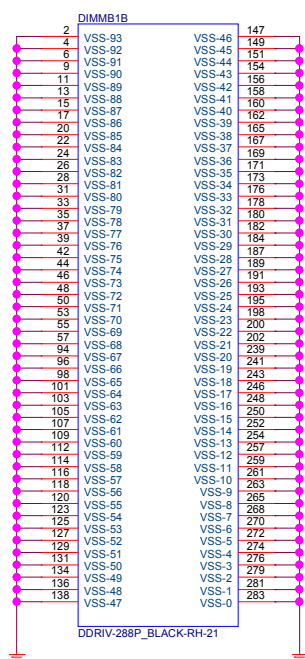
DIMM SLOT PN BY SPEC



DDR VREF

(place resistors close to DIMMs)





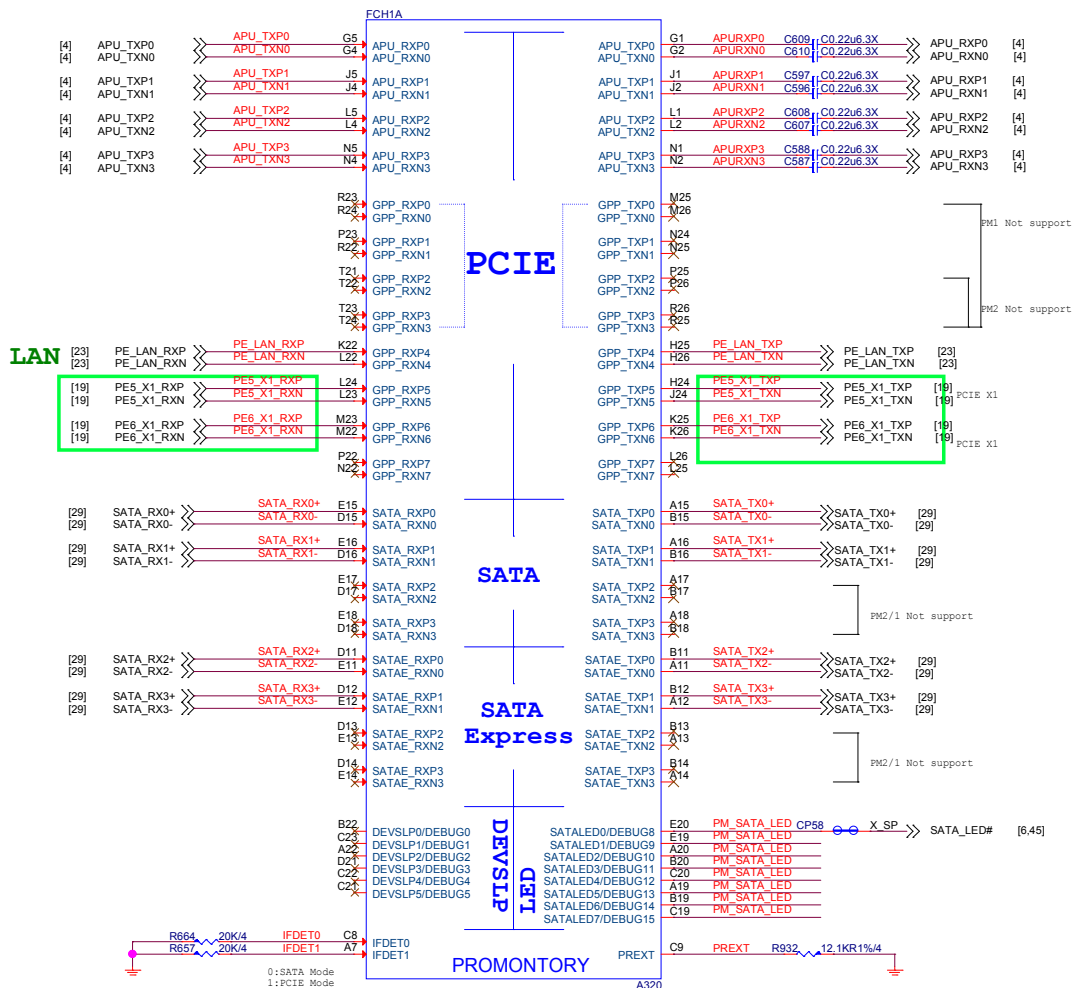
PCIE

SATA

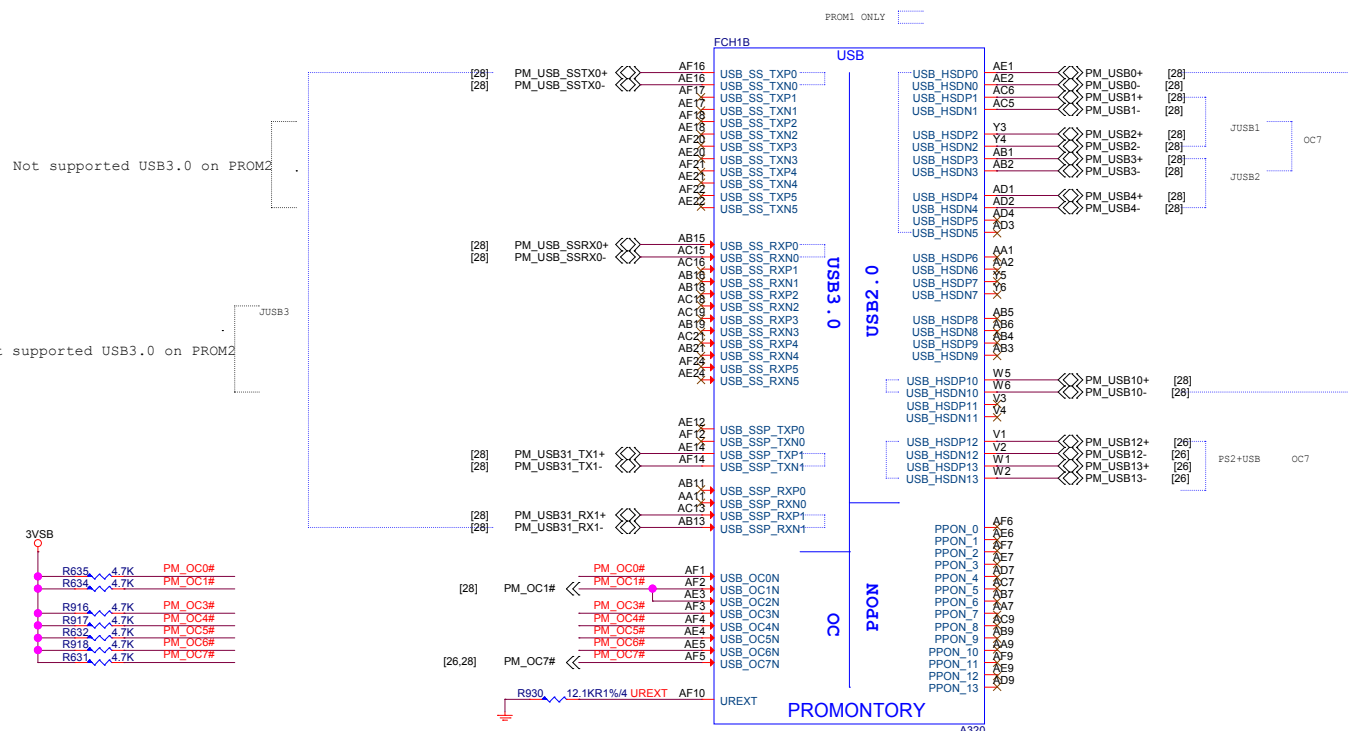
SATA Express

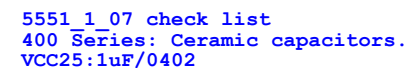
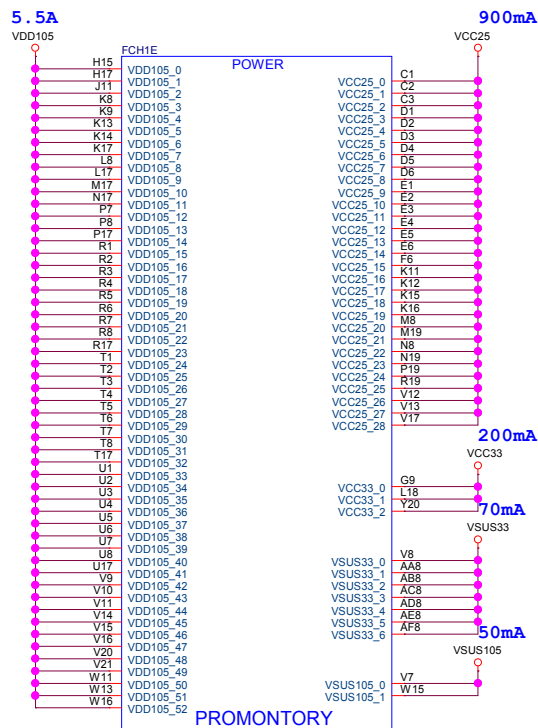
DEVSLP LED

PROMONTORY



SATA Express port0 (IFDET0)
SATA Express port1 (IFDET1)
0:SATA Mode
1:PCIE Mode



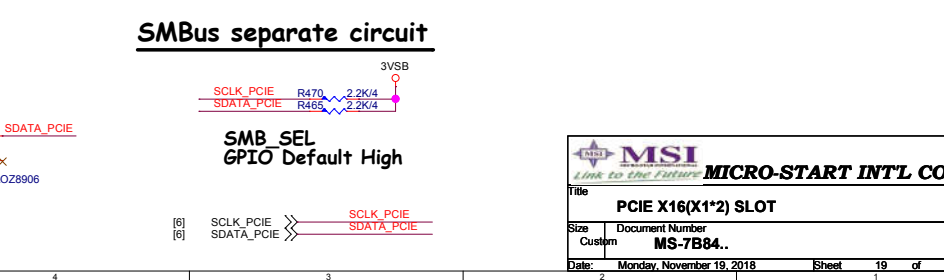
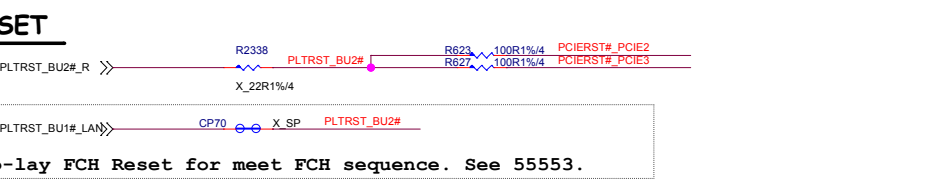
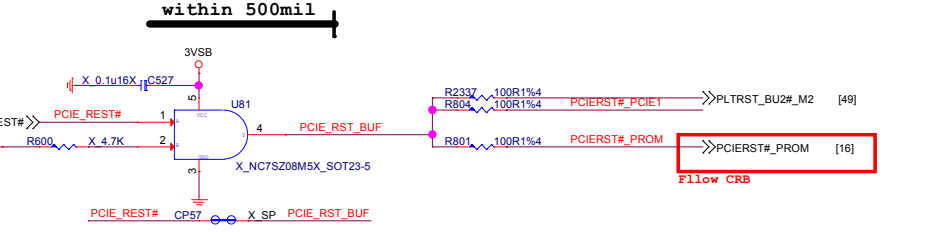
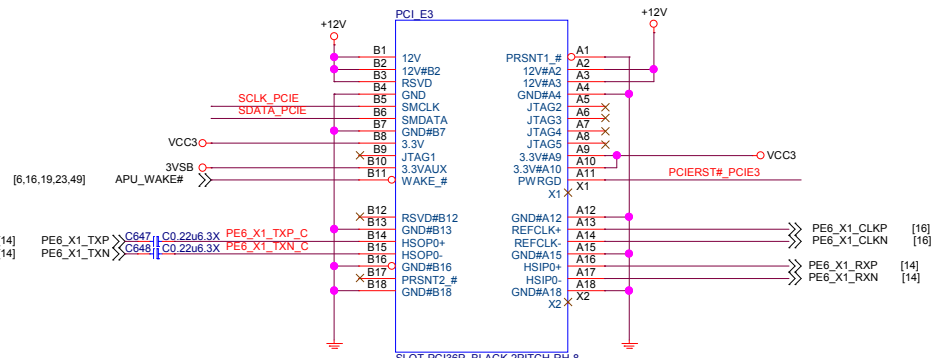
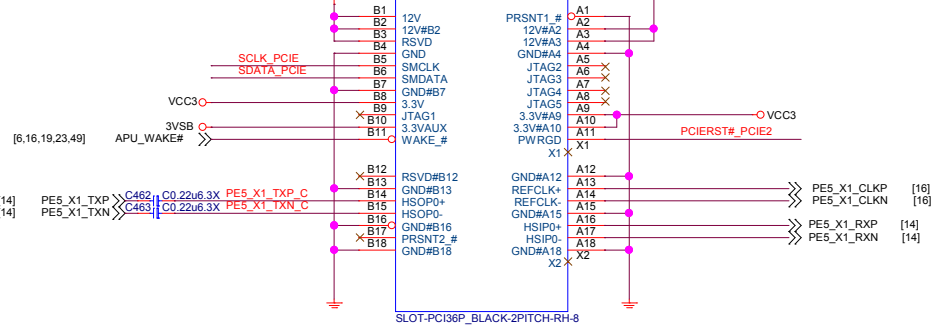
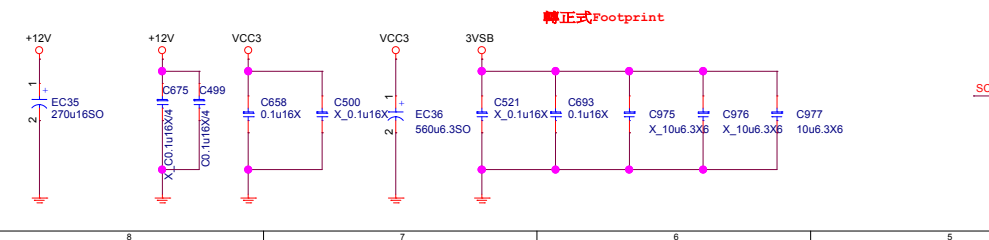
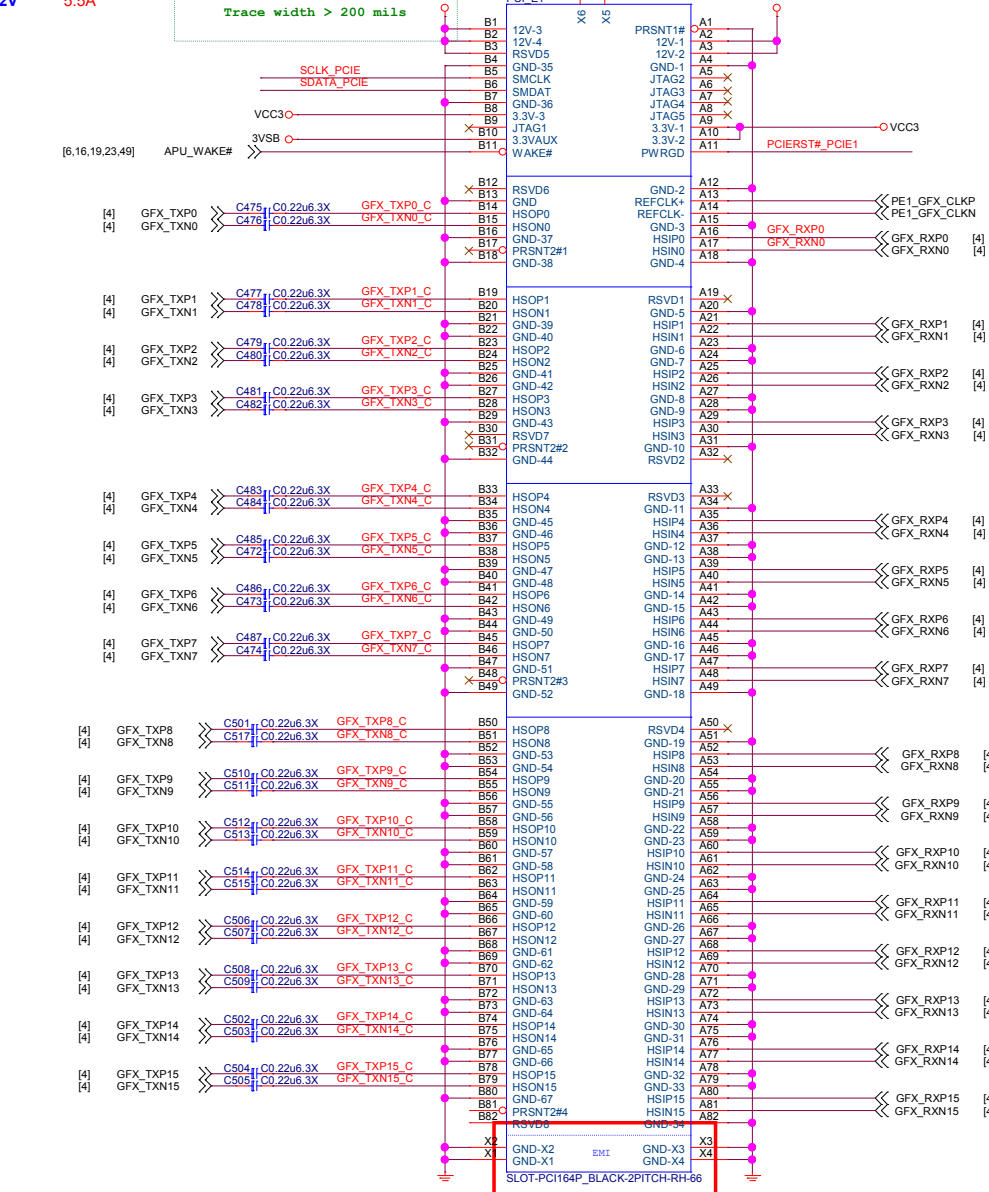


PCI EXPRESS x16 Slot

3.3V 12V 3.0A 5.5A

PCIEX1 12V 0.5A 3.3V weak 375mA

3.3V 12V 3.0A 0.5A



MSI MICRO-START INT'L CO.,LTD.

Title: PCIE X16(X1*2) SLOT

Size: Custom

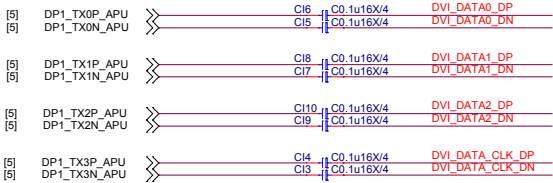
Document Number: MS-7B84..

Date: Monday, November 19, 2018

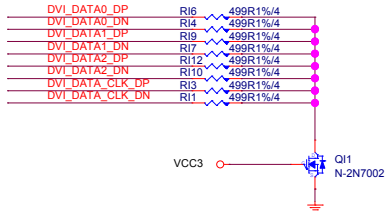
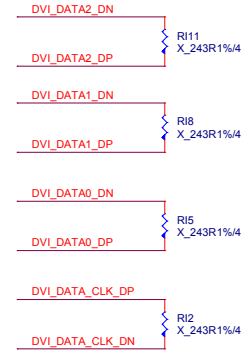
Sheet: 19 of 53

Rev: 20

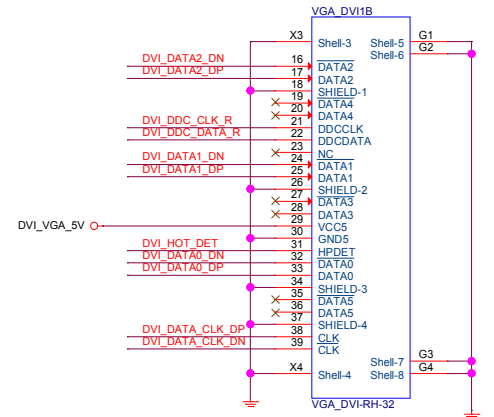
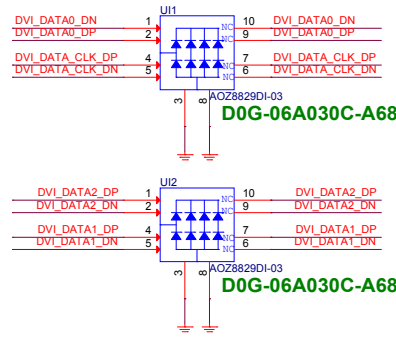
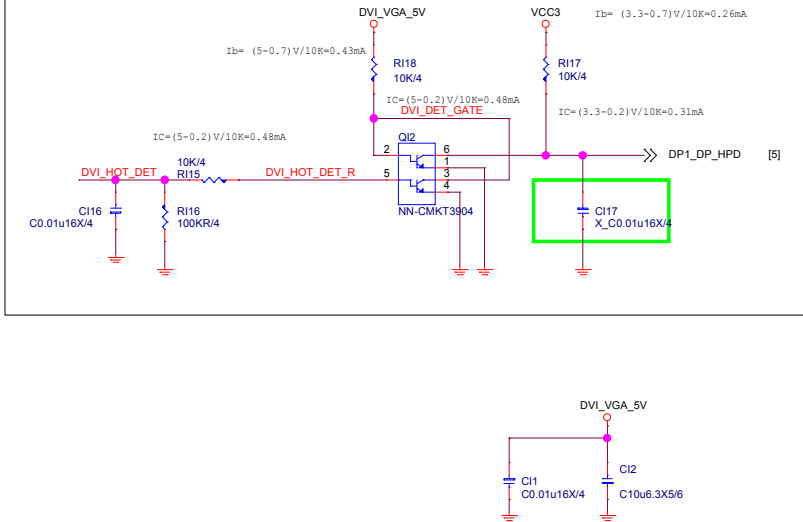
DVI CONNECTOR



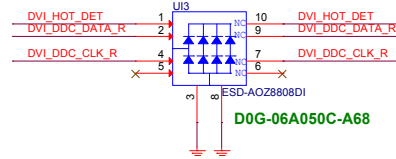
For EMI



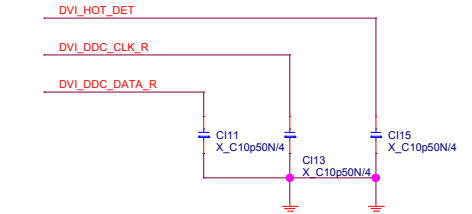
HPD



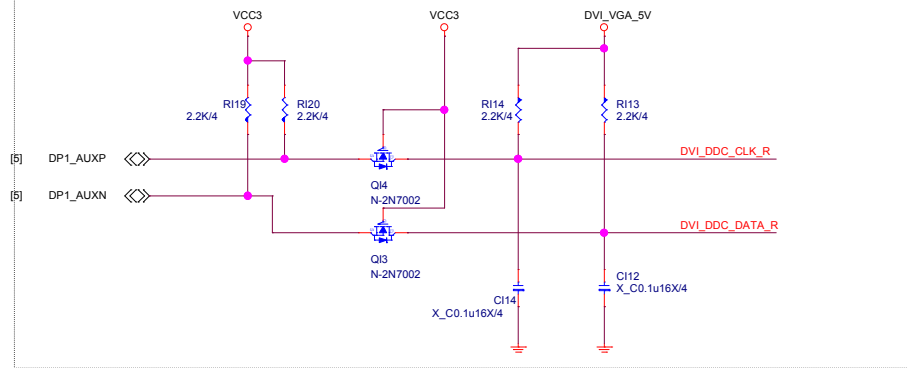
注意:耐壓5v零件



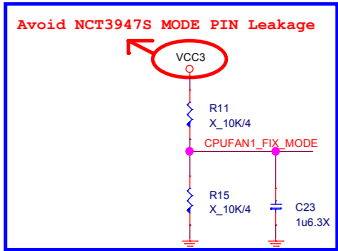
For EMI



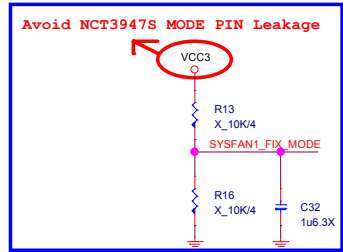
LEVEL SHIFT using I2C Repeater



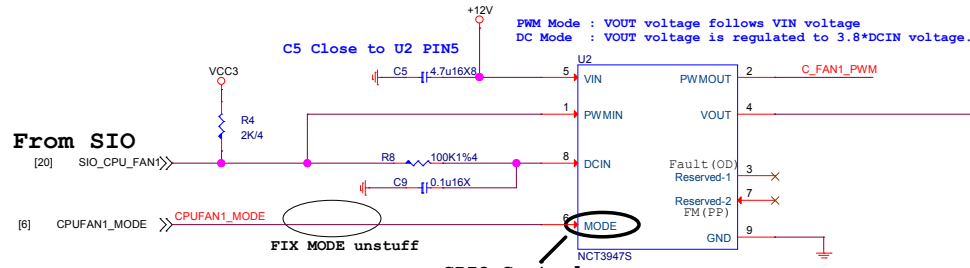
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE
2.GPIO可以由BIOS切换 PWM/DC MODE



Resever For FIX DC or PWM MODE USE By PM SPEC



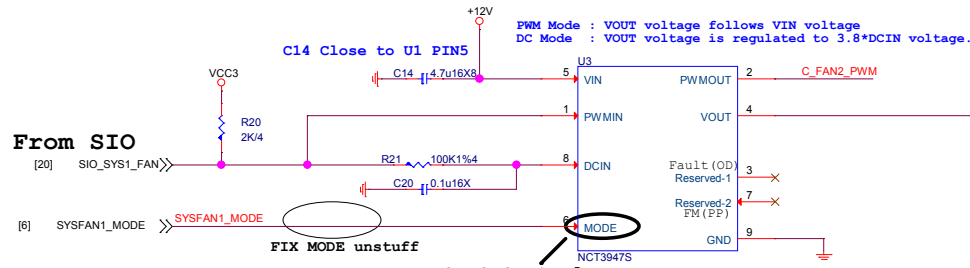
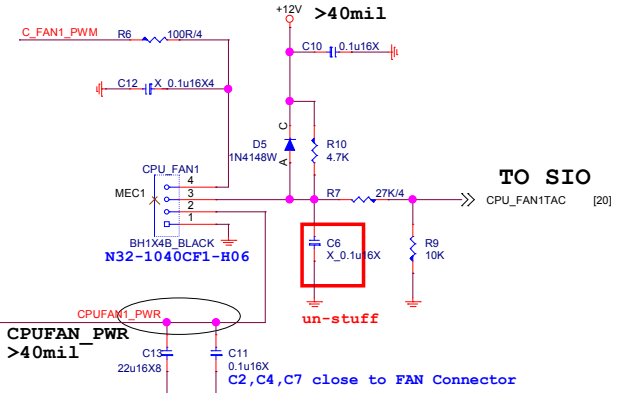
Resever For FIX DC or PWM MODE USE By PM SPEC



GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

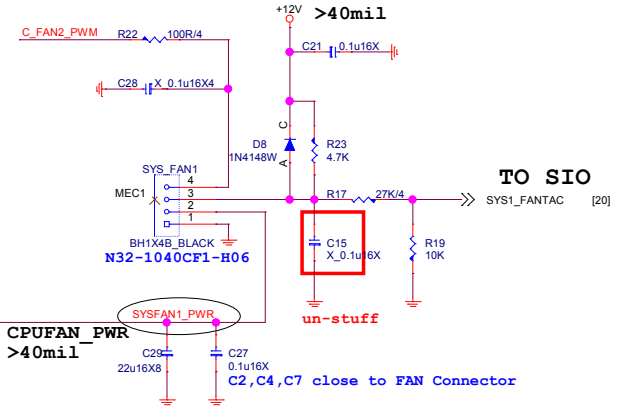
Default Internall pull up 1.65V



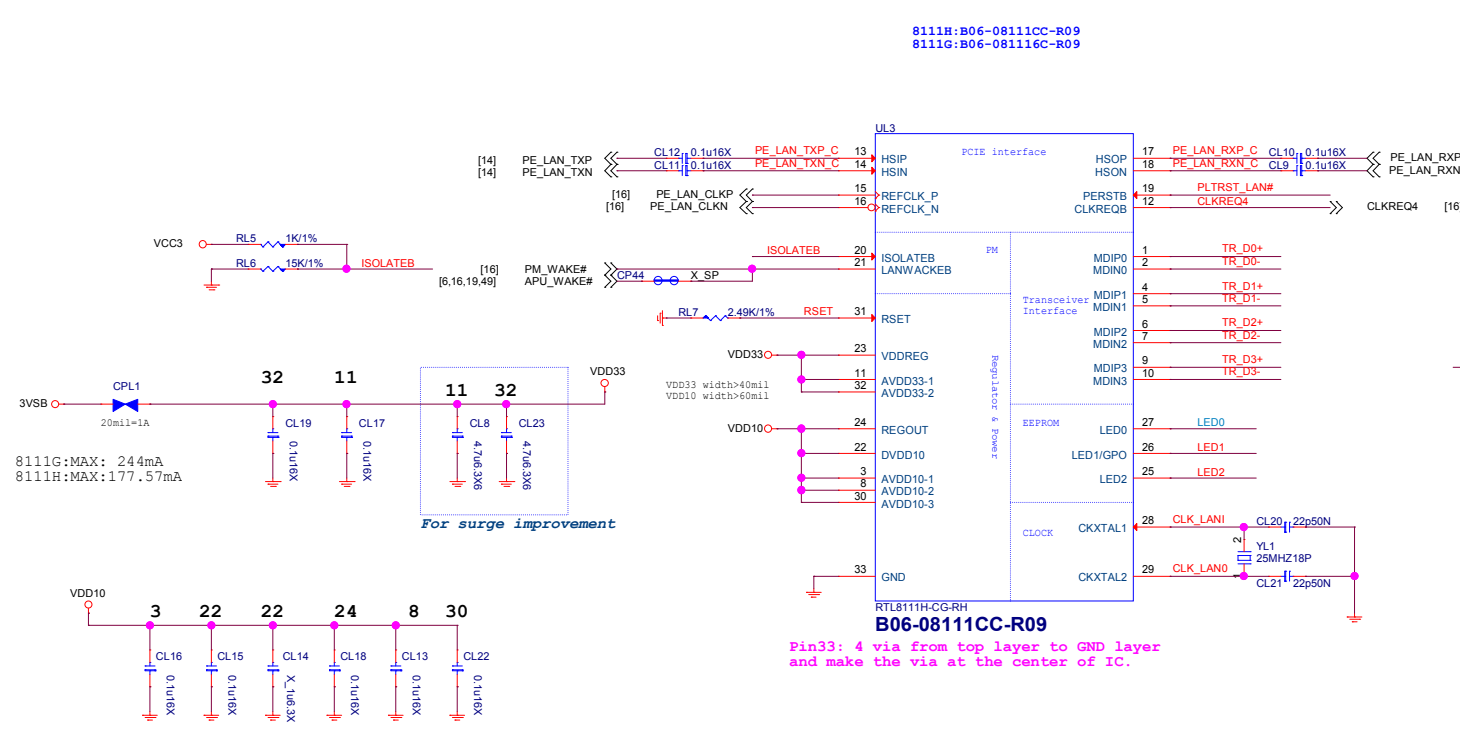
GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default Internall pull up 1.65V



RTL8111G/RTL8111H Giga LAN

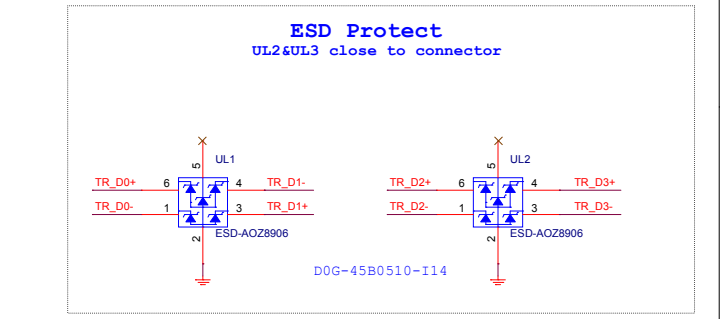
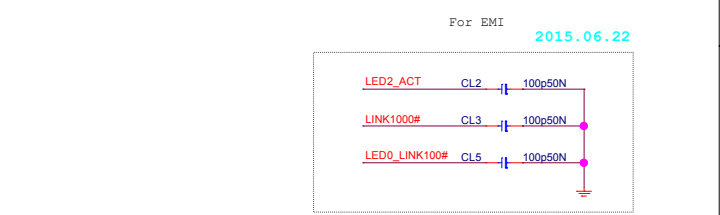
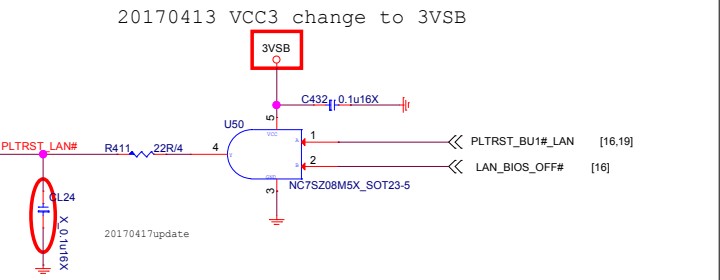
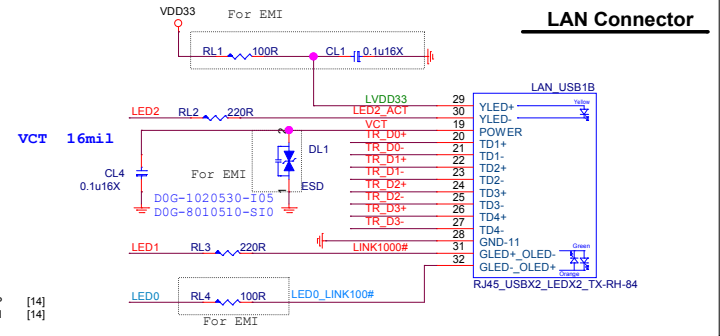


8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



MSI MICRO-START INT'L CO.,LTD.

Title: LAN-RTL8111H

Size: Custom

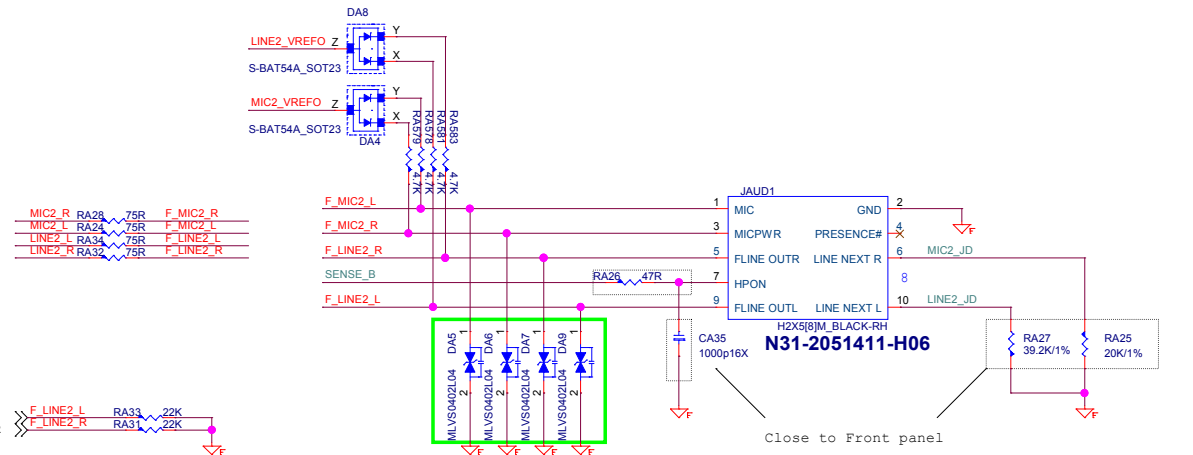
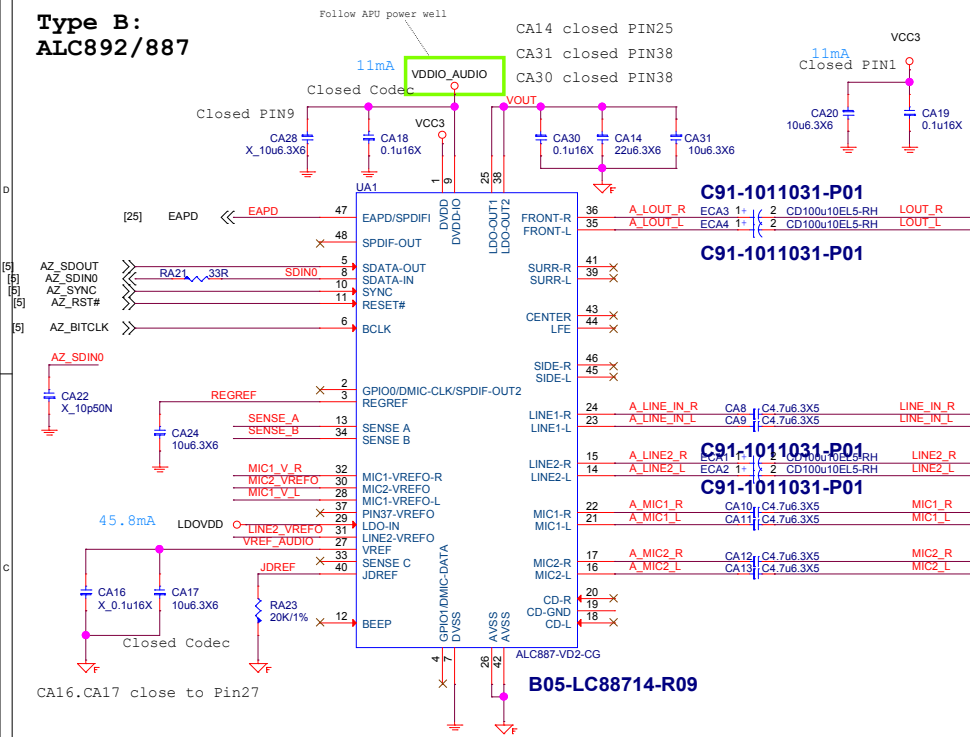
Document Number: MS-7B84..

Date: Monday, November 19, 2018

Sheet: 23 of 53

Rev: 20

Type B:
ALC892/887

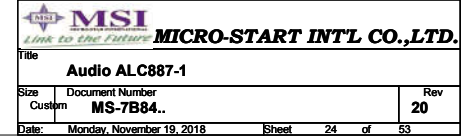


Close to Front panel
For HDA/AC97 front cable.

Varister --> cap for cost down

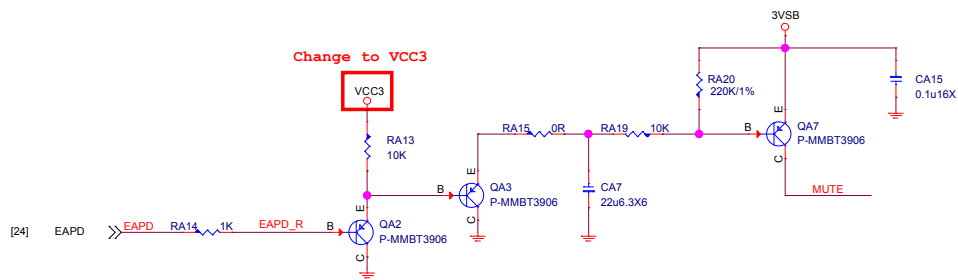
D0G-2710510-I05

Close to Jack



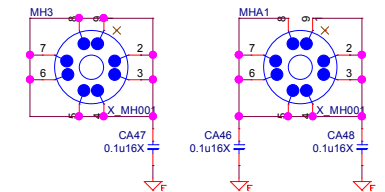
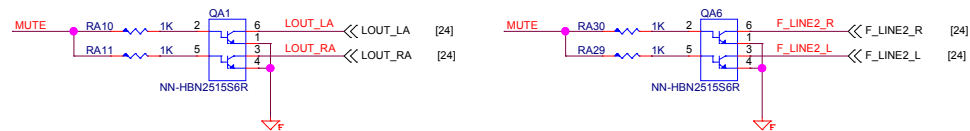
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

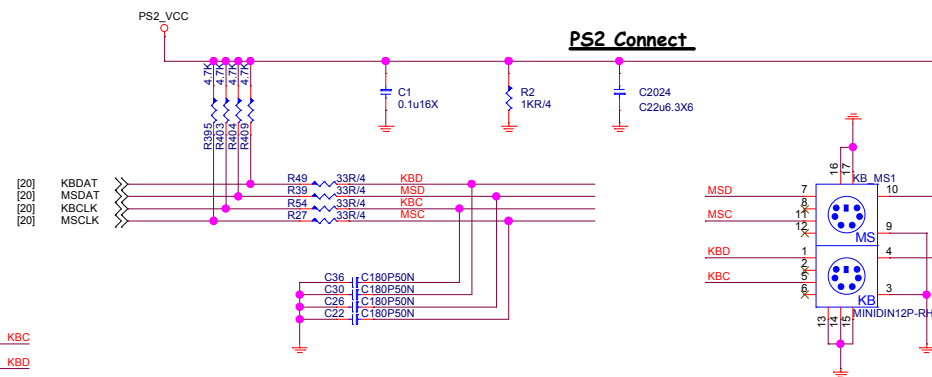


Digital

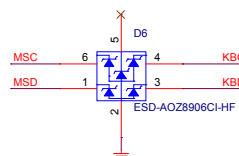
Analog



PS2+USB



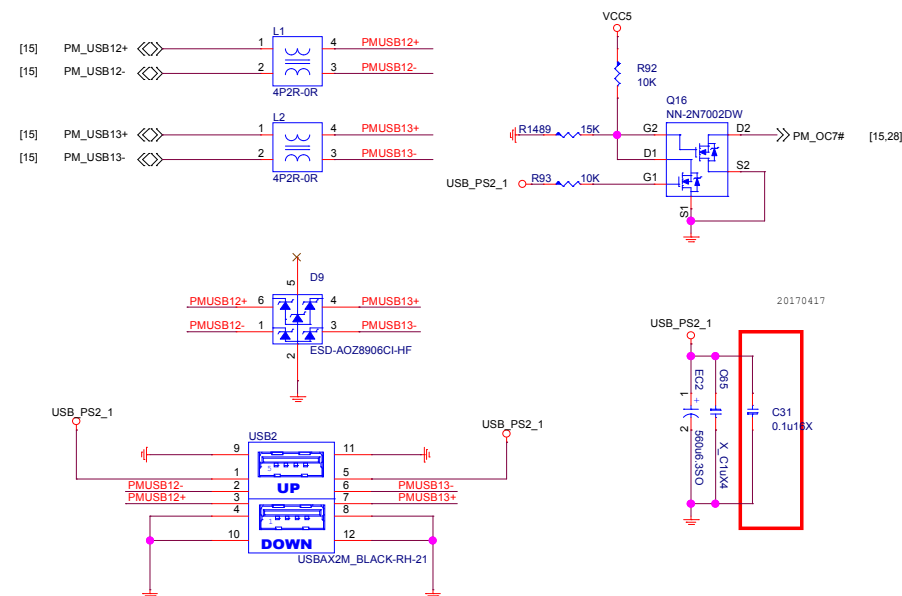
TVS P/N:
D0G-45B0510-I14



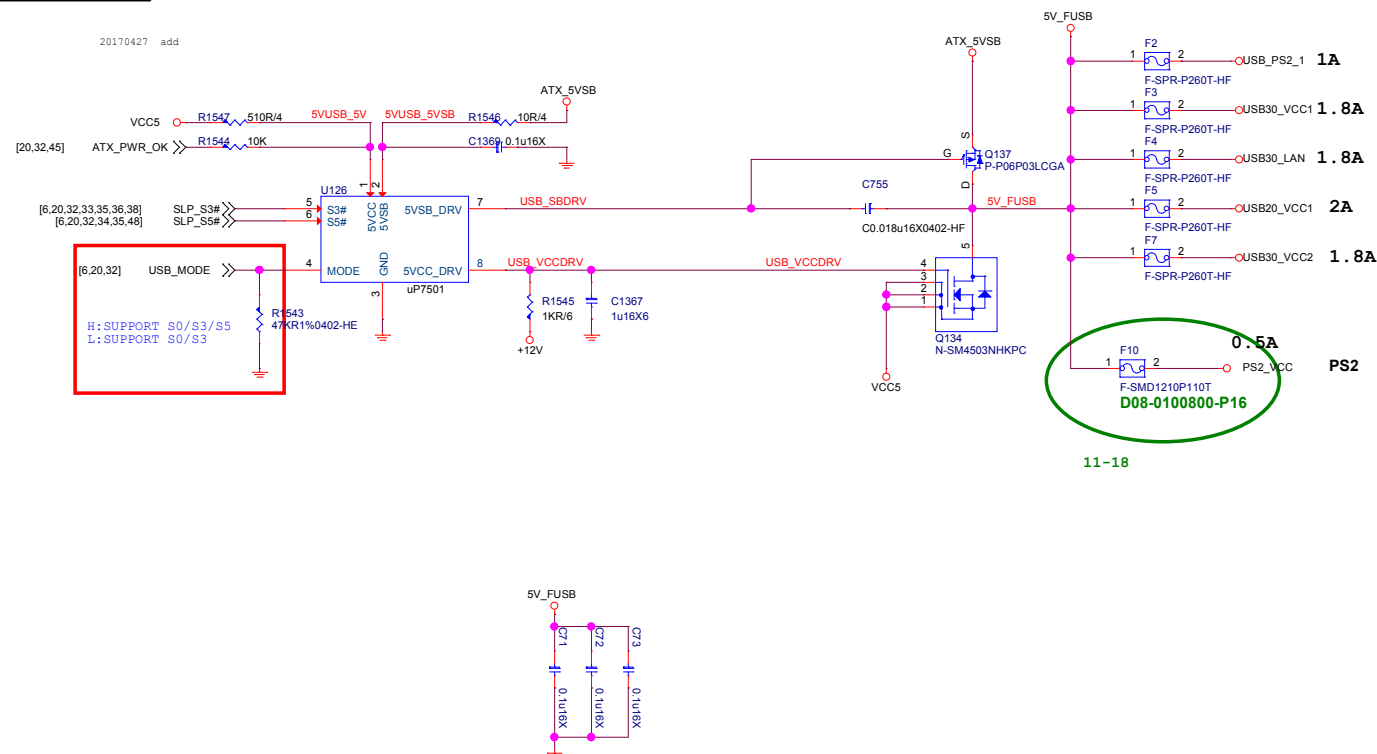
```

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

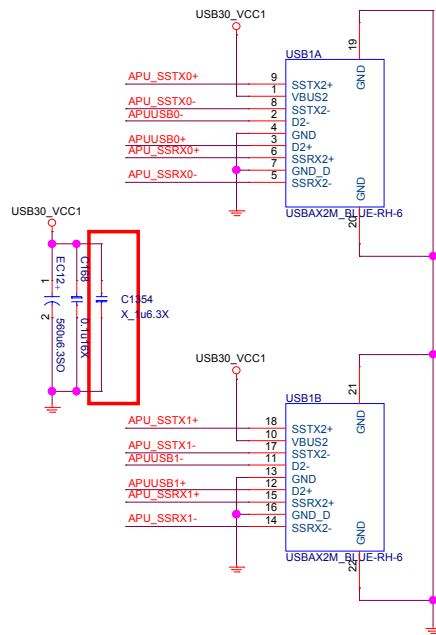
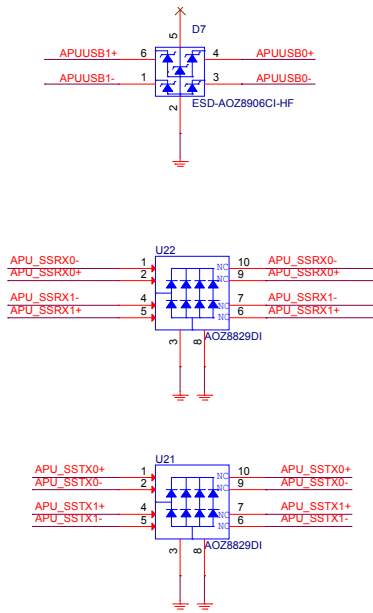
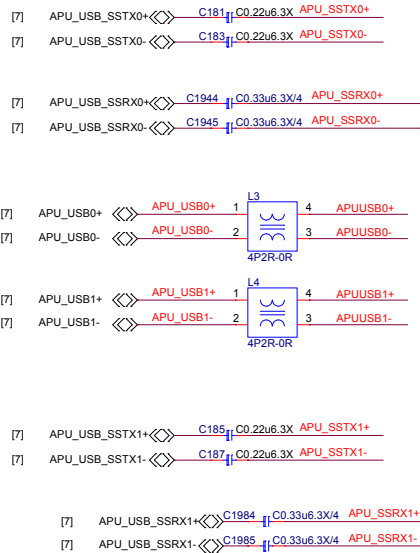
```



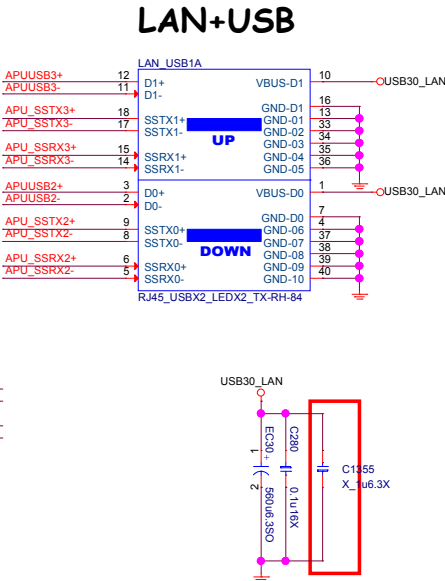
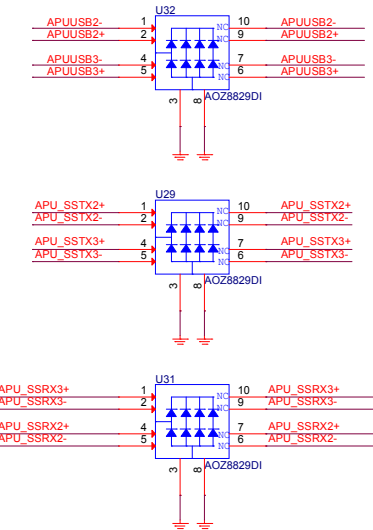
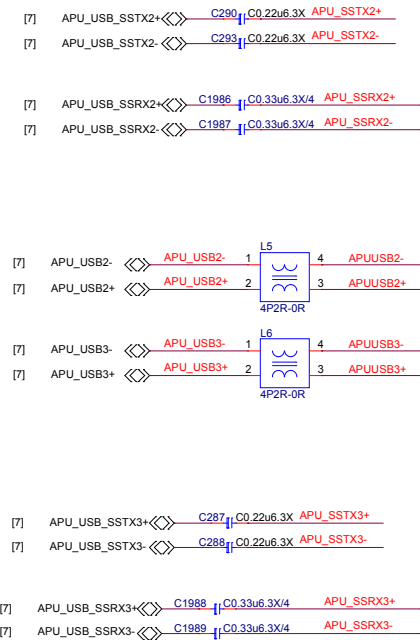
USB Power



USB 3.0

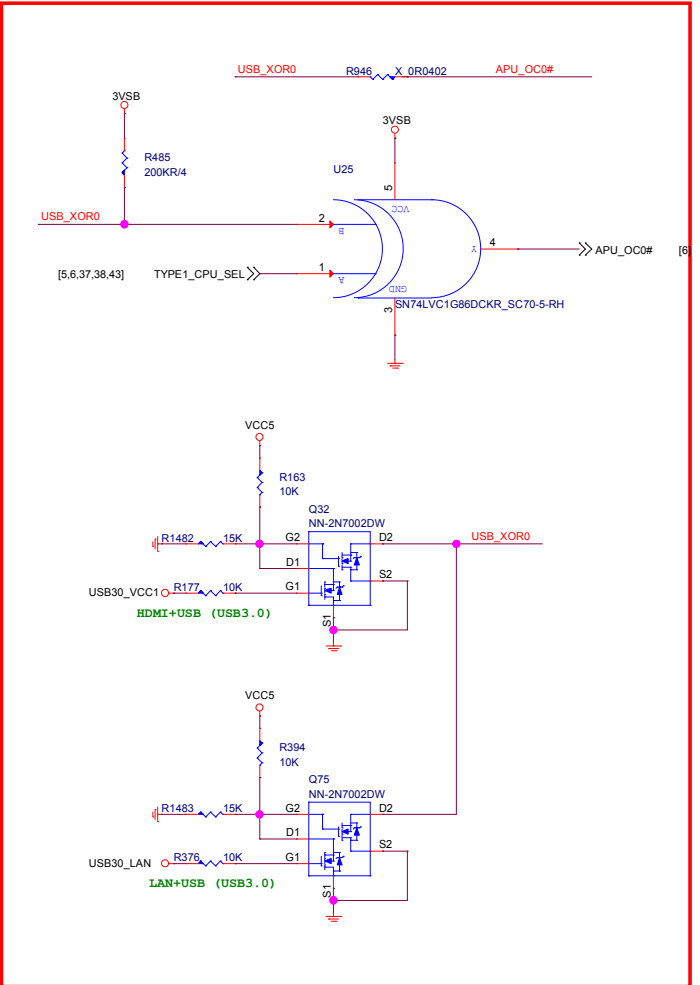


USB3.1 GEN1



APU_USB_OC

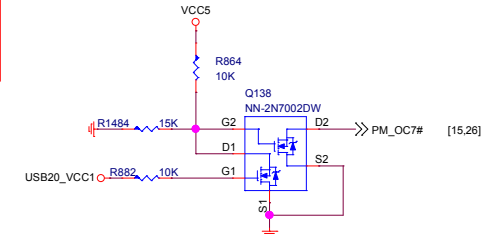
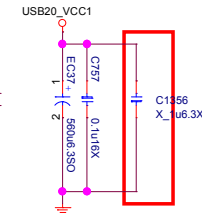
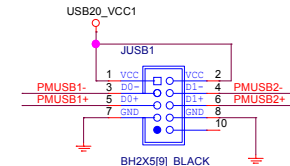
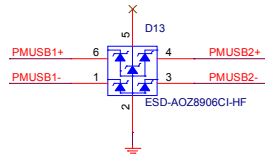
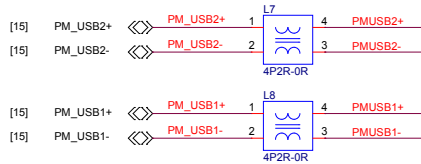
Modify USB_OC# circuit



	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

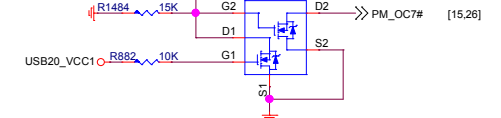
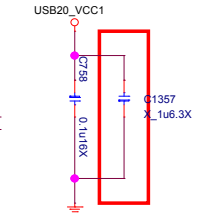
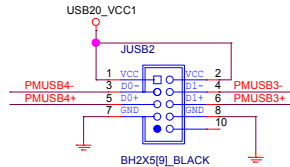
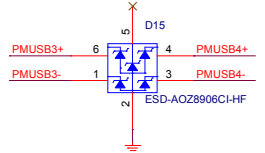
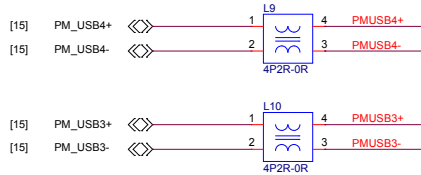
Front USB2.0 (JUSB1)

5V@1A

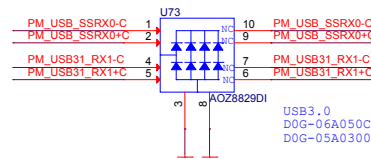
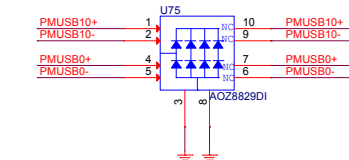
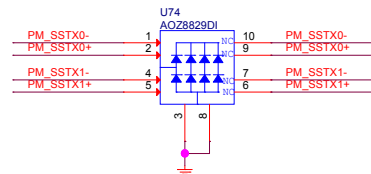
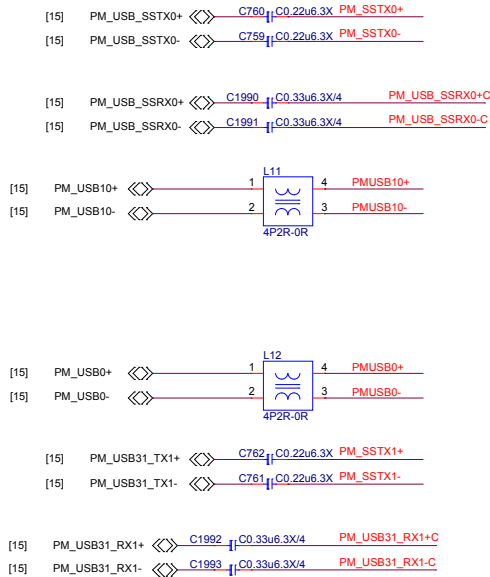


Front USB2.0 (JUSB2)

5V@1A

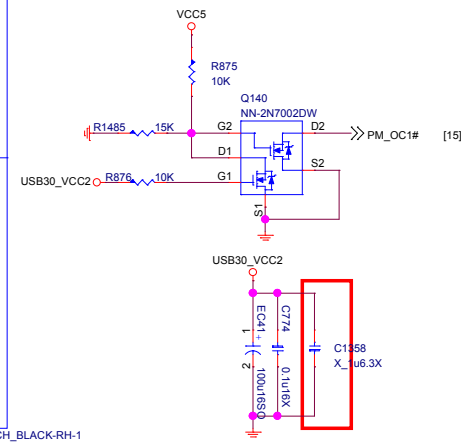
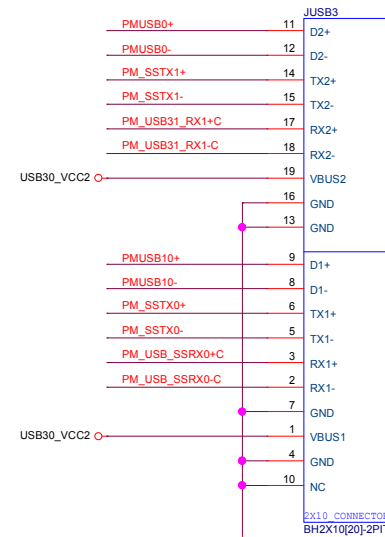


Front USB3.1 GEN1

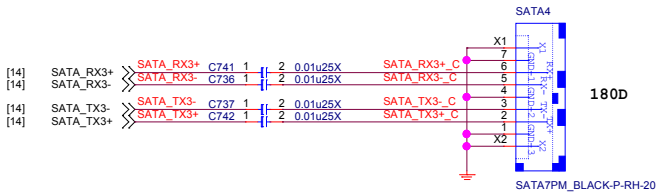
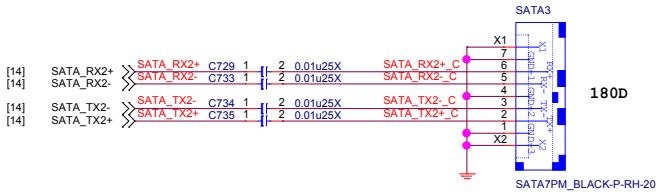
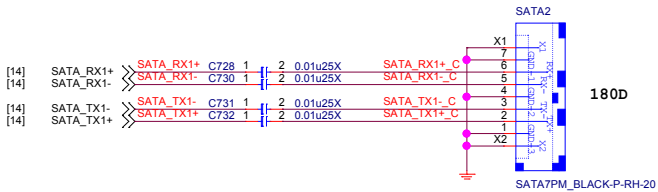
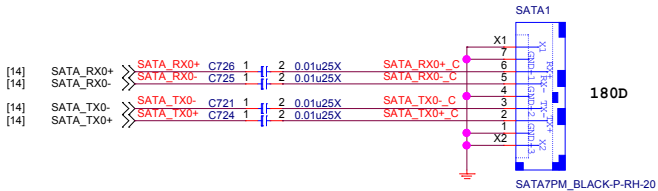


USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL

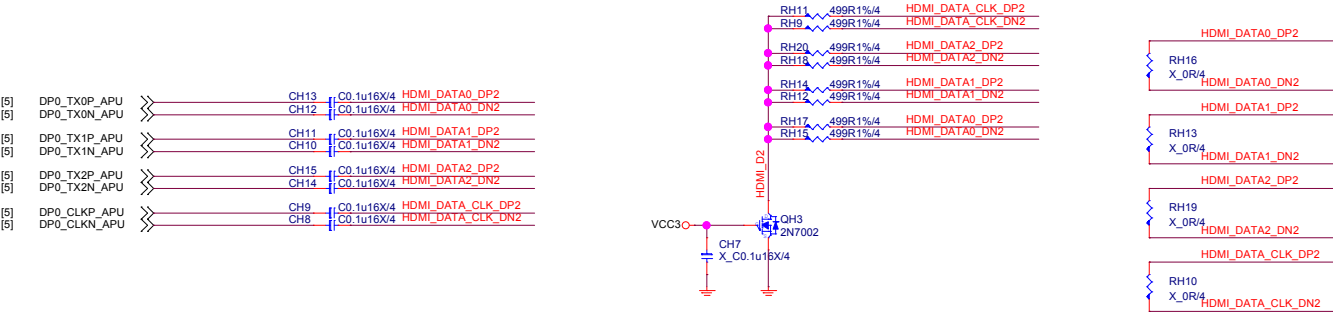


SATA Connector

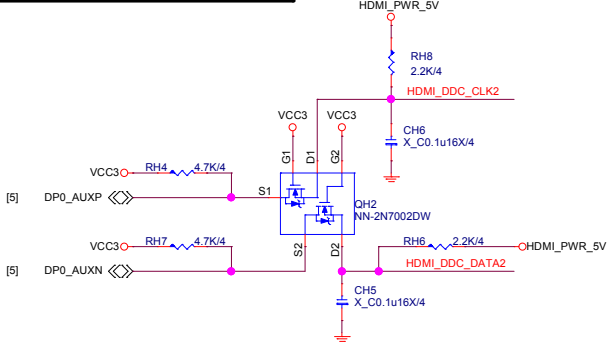


HDMI CONNECTOR

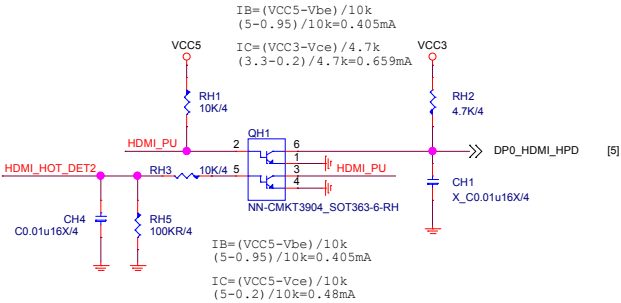
For HDMI 1.4



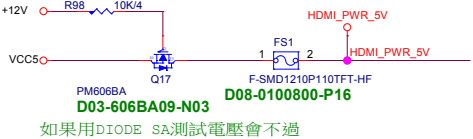
AUX Level Shifter



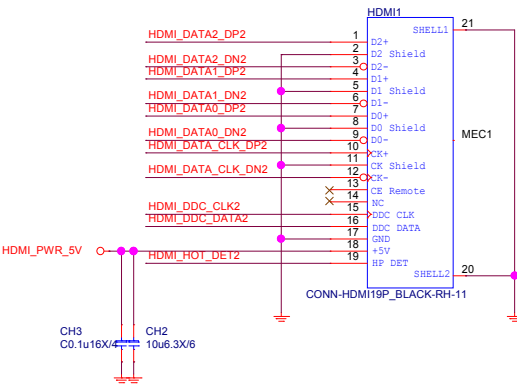
HPD Circuit



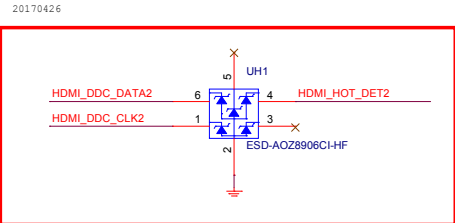
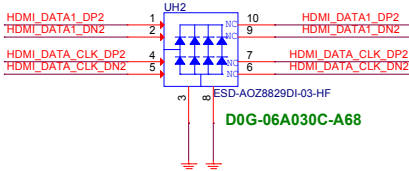
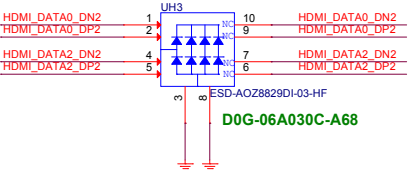
Connector Power



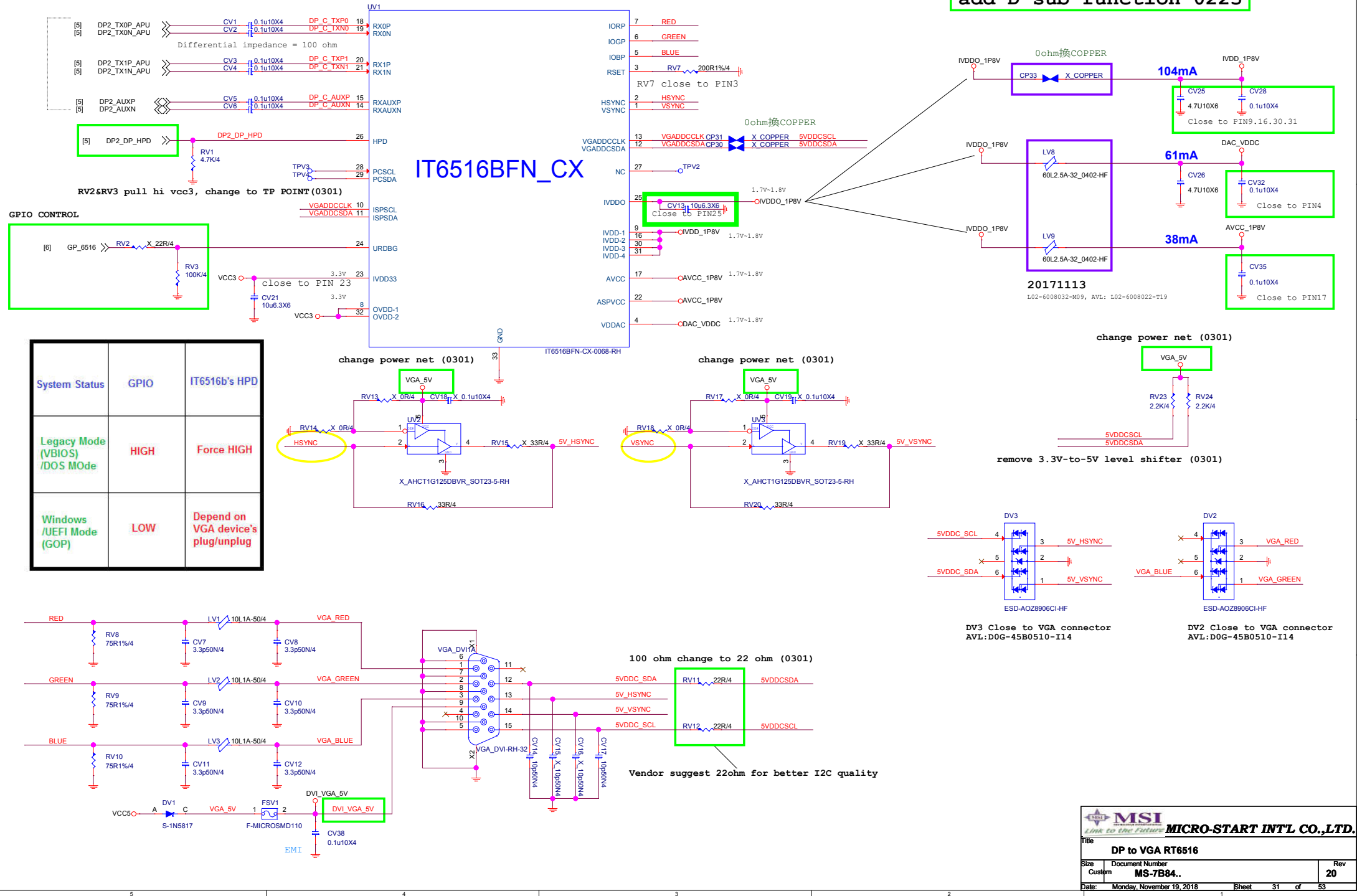
Connector



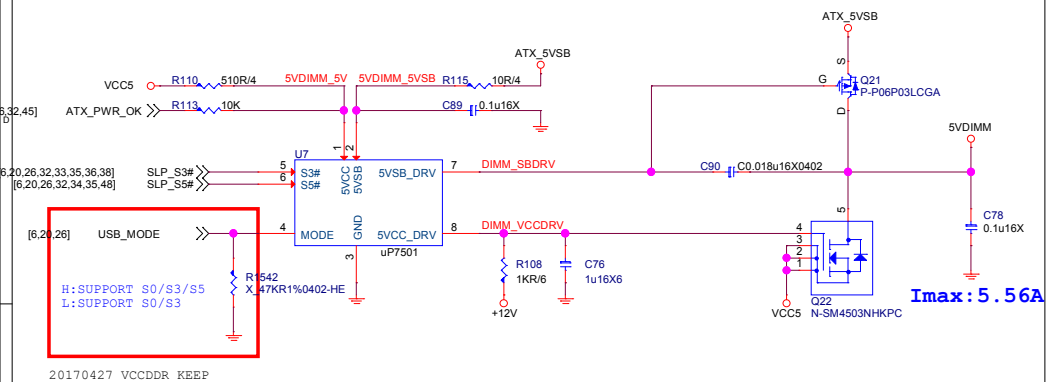
For EMI



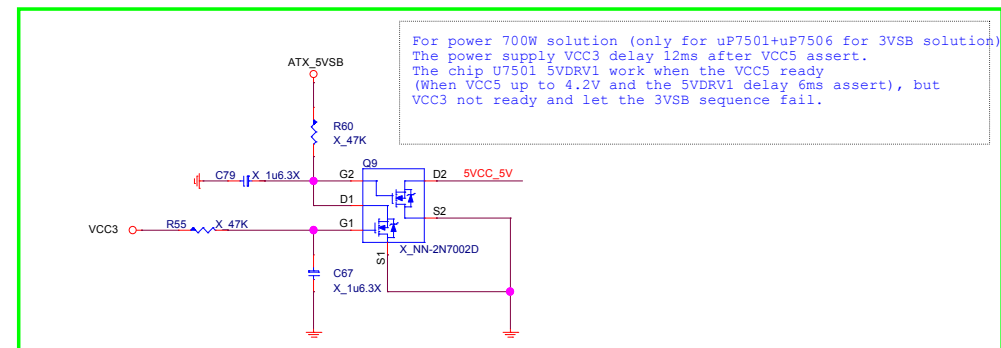
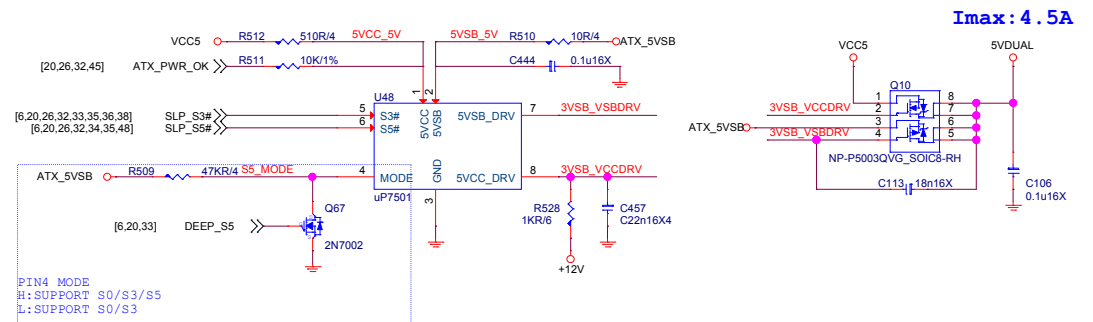
Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



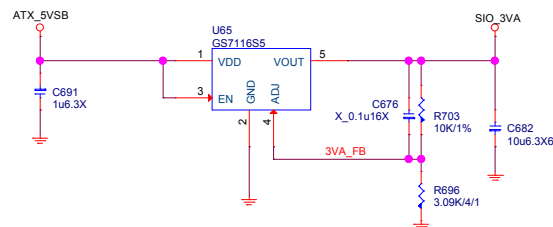
5VDIMM FOR DDR



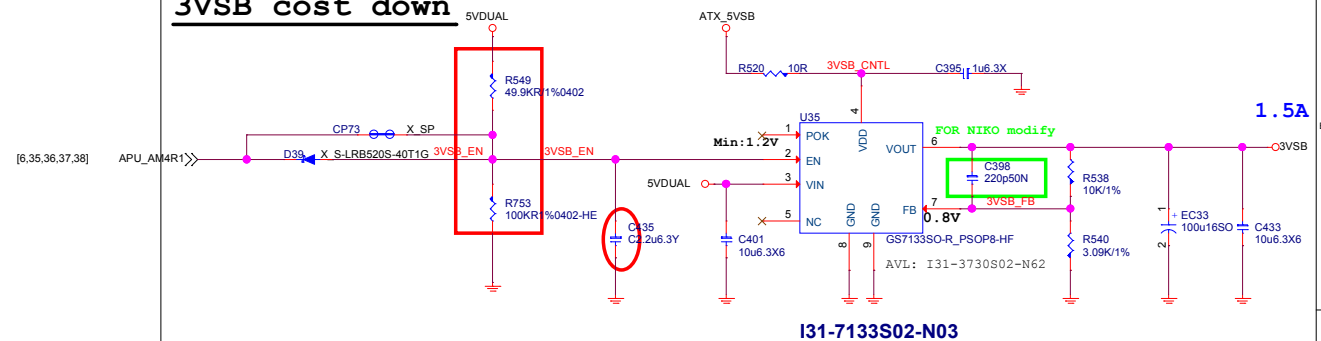
5VDUAL For 3VSB、CPU 1.8V、VDDP



SIO_3VA

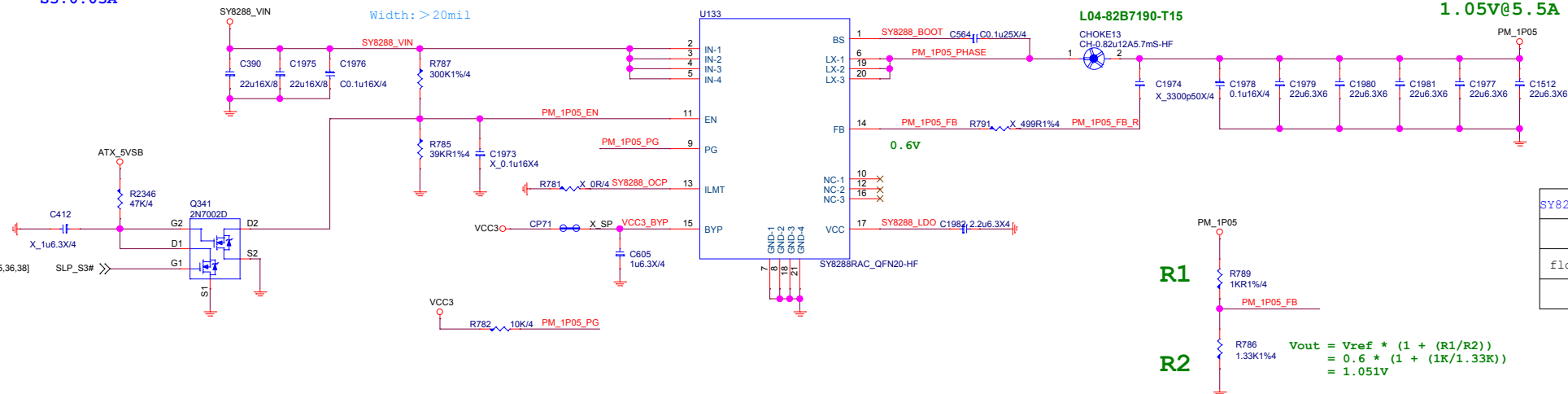


3VSB cost down



1.05V
S0:5.5A
S5:0.05A

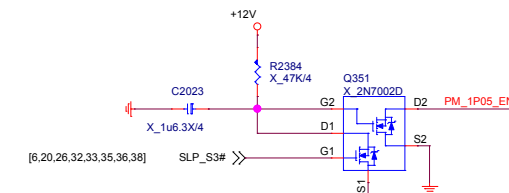
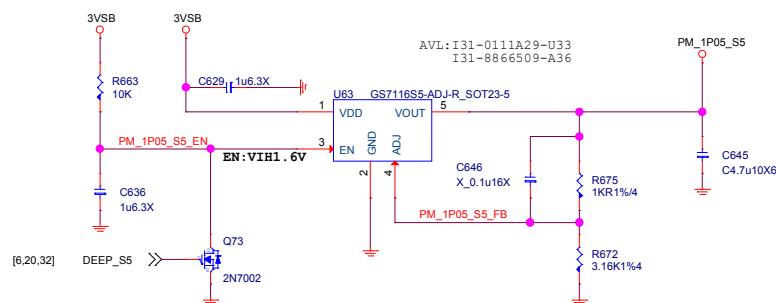
OCP=12A
1.05V@5.5A



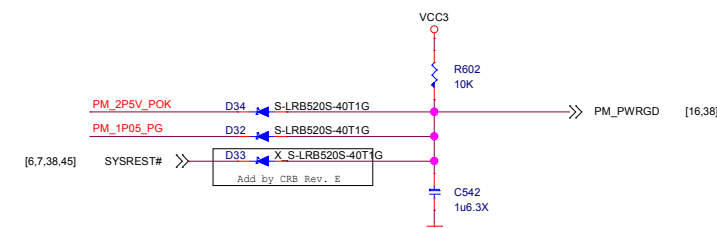
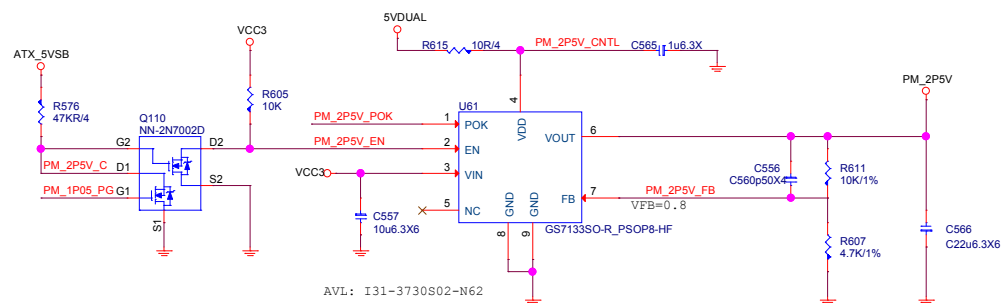
SY8288_OCP	OCP
0	8A
floating	12A
1	16A

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (1K/1.33K)) \\ &= 1.051V \end{aligned}$$

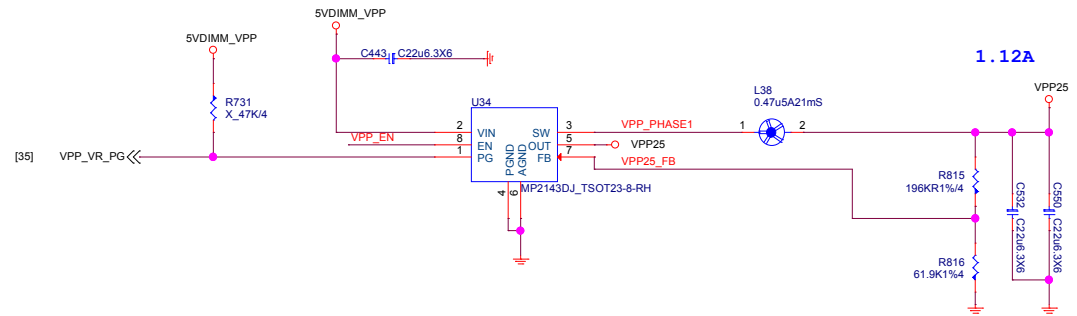
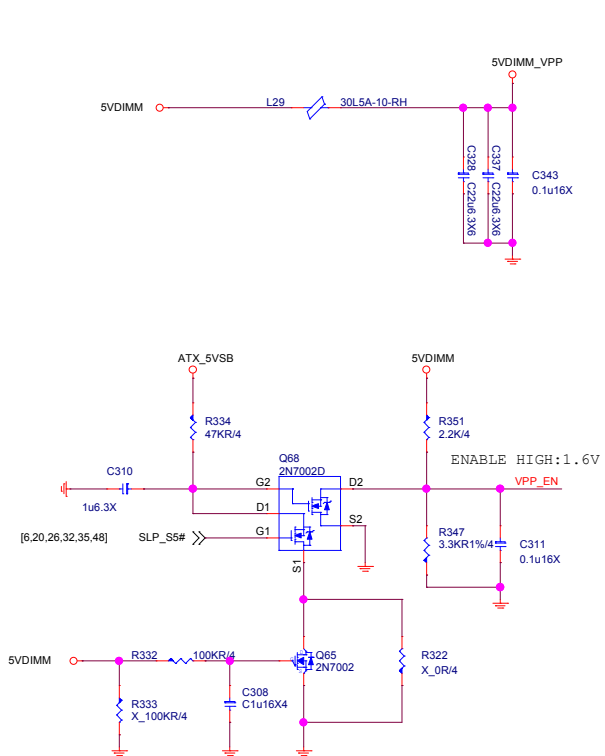
0.05A



2.5V; 900mA

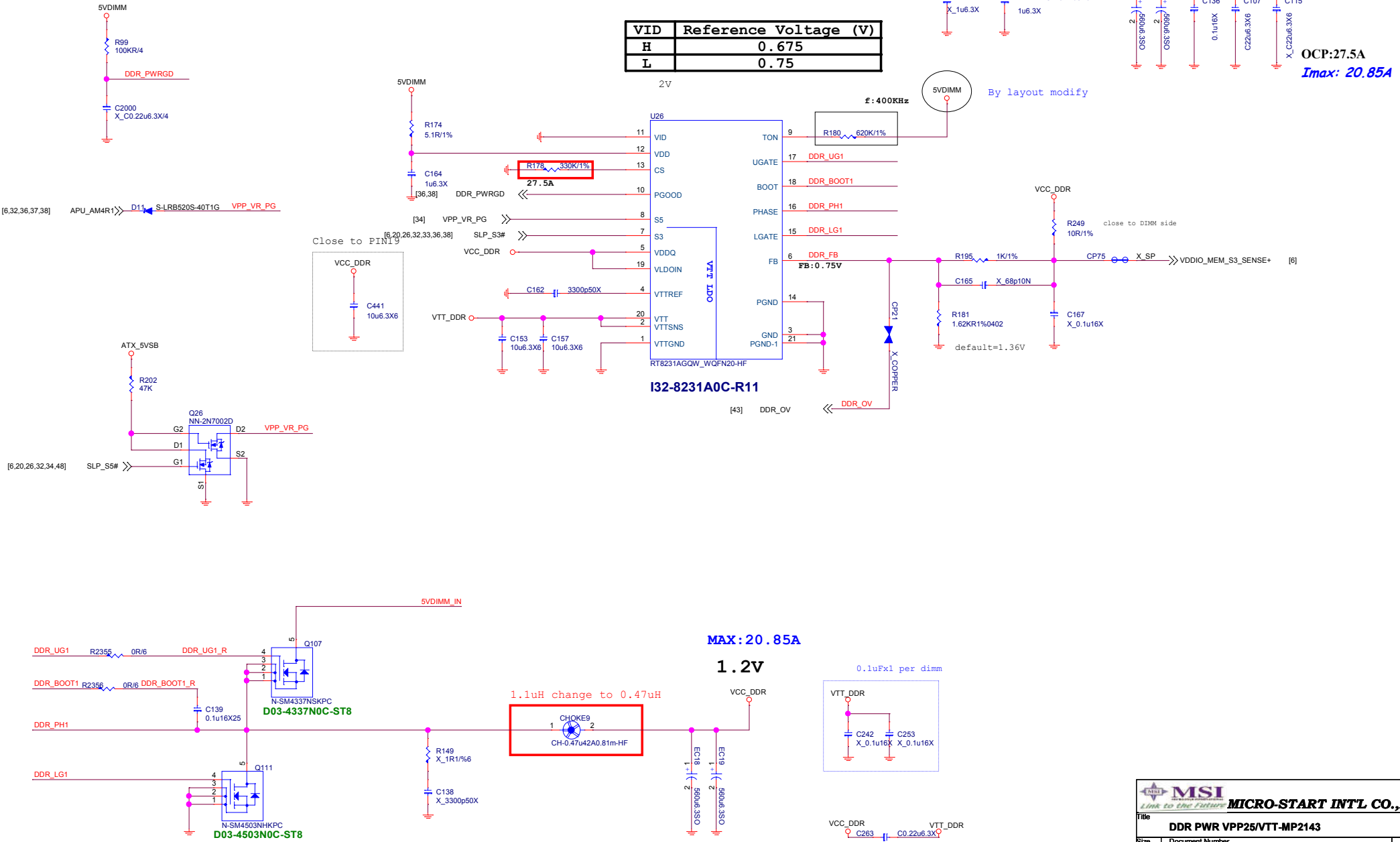


2DIMM :1.12A FOR DDR VPP2.5V



DDR4_1.2V 15.5A+4.75A+0.6A=20.85A
15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT

$I_{rms} = I_{out} * \sqrt{D/N - (D)^2}$
VCCDDR:
 $D = V_{out}/V_{in} = 1.2/5 = 0.24$
 $N = \text{Phase number} = 1$
 $= 20.85A * \sqrt{0.24 - 0.0576}$
 $= 5.21A$



OCP:27.5A
I_{max}: 20.85A

MAX: 20.85A
1.2V

FOR CPU 1.8V S5

0.5A

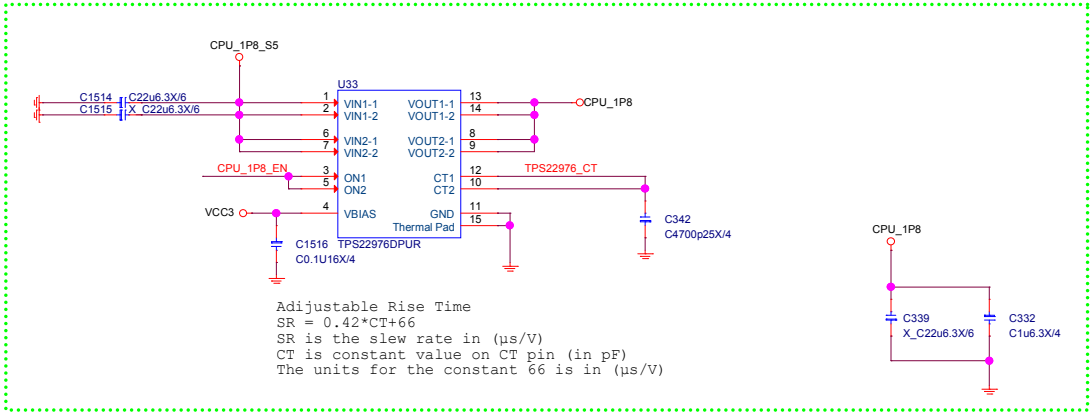
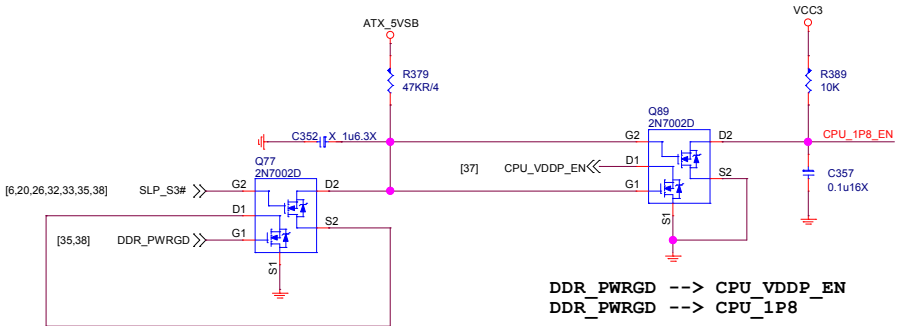
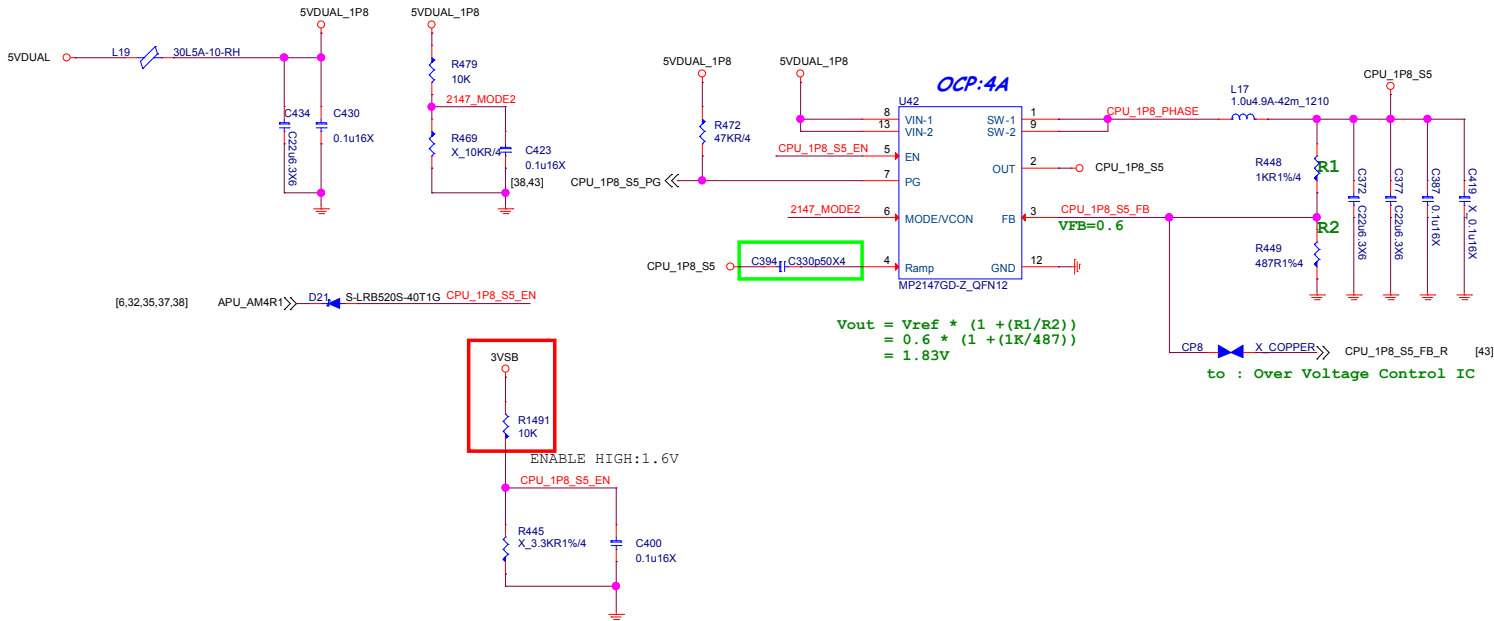
FOR VCCP_SOC_S5

0.9A

FOR CPU 1.8V S0

2.0A

0.5A + 2.0A +
0.9A = 3.4A



CPU_VDDP_S0

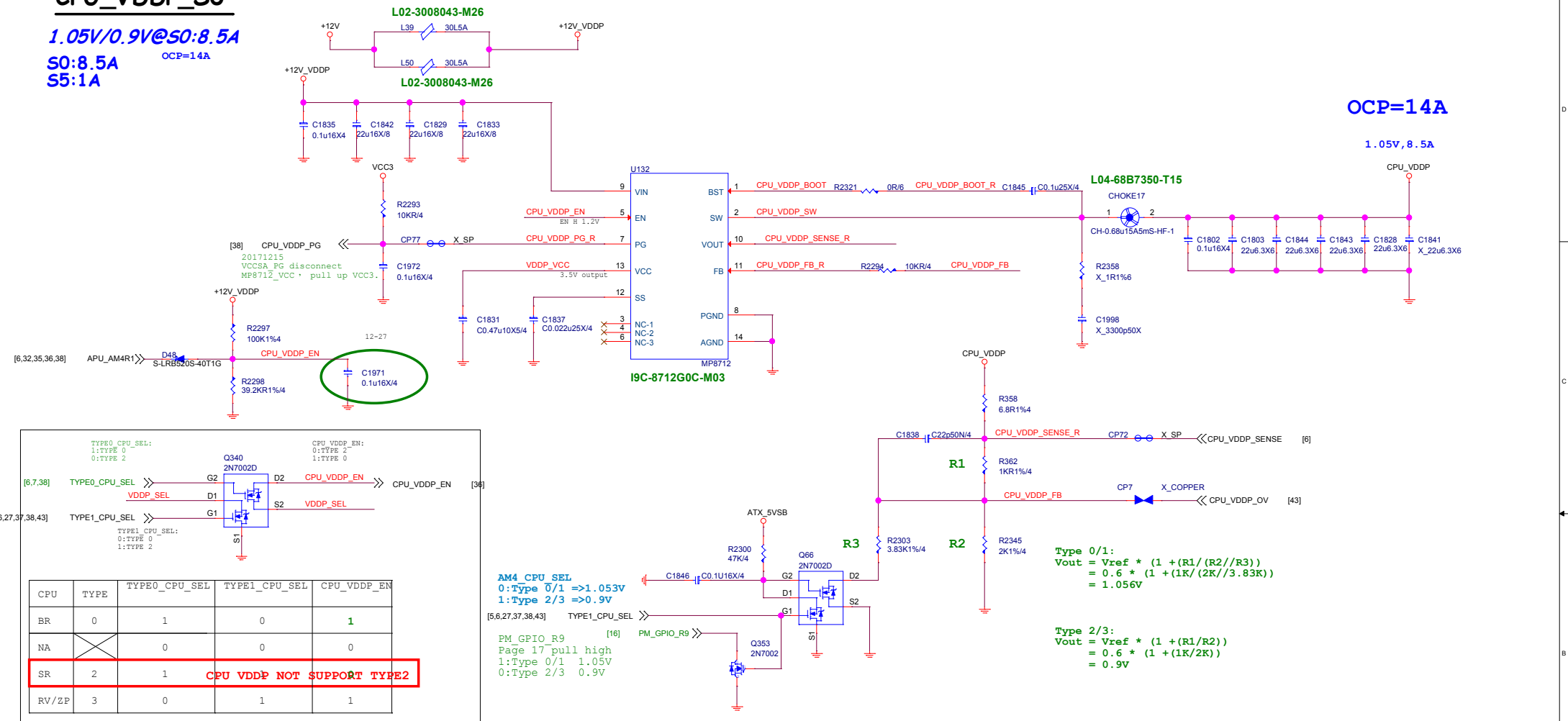
1.05V/0.9V@S0:8.5A
S0:8.5A
S5:1A

OCP=14A

Input Current= (8.5A*1.05V)/12V/0.8=0.93A

OCP=14A

1.05V, 8.5A

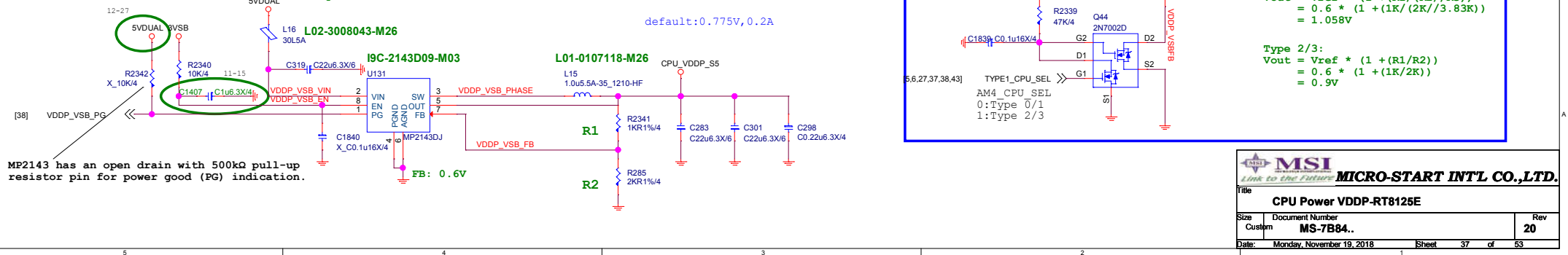


CPU_VDDP_S5

1.05V/0.9V
S5:1A

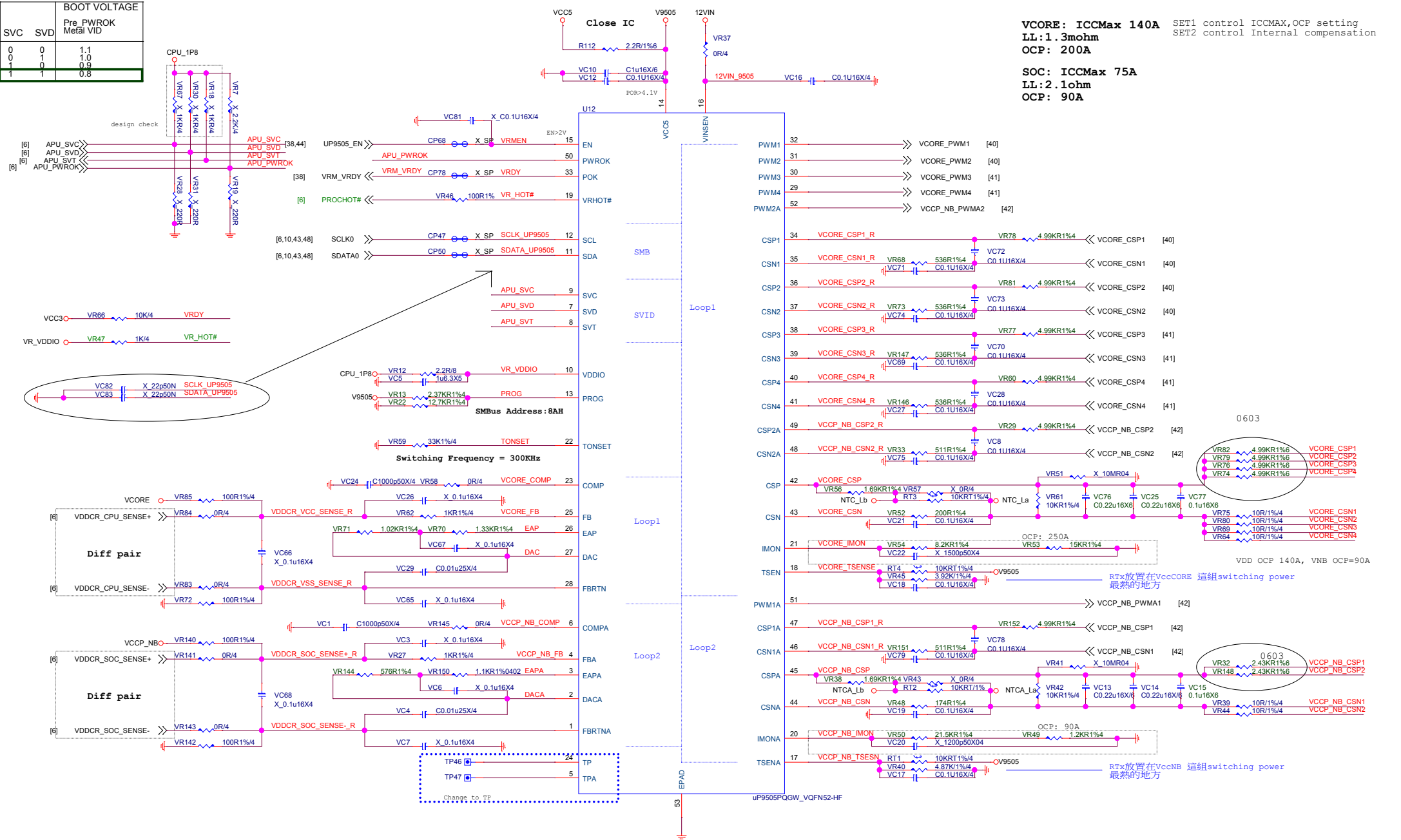
Input Current=0.04A

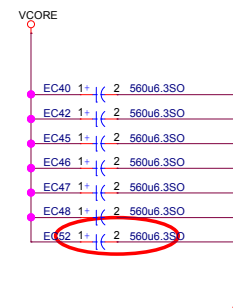
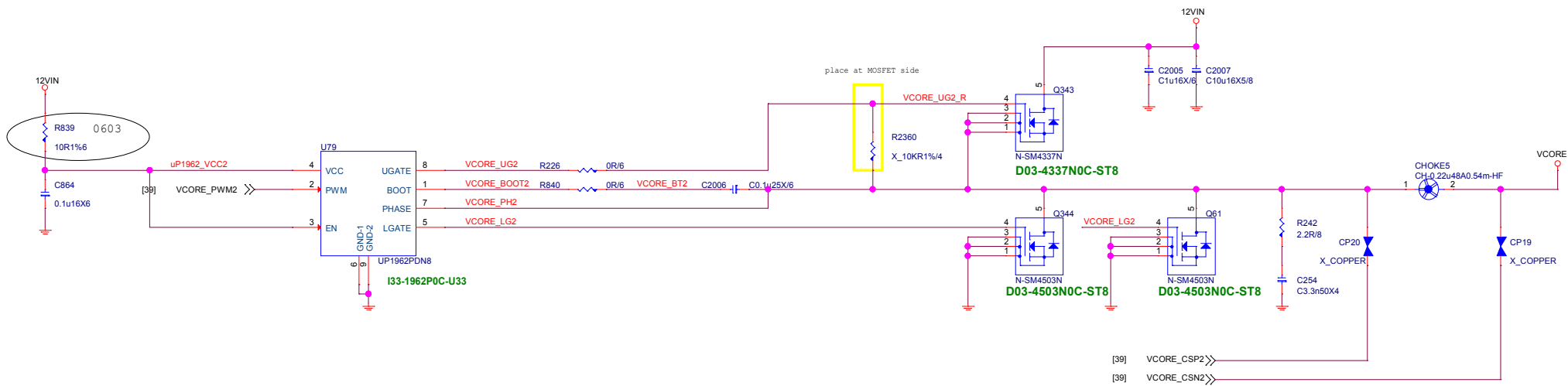
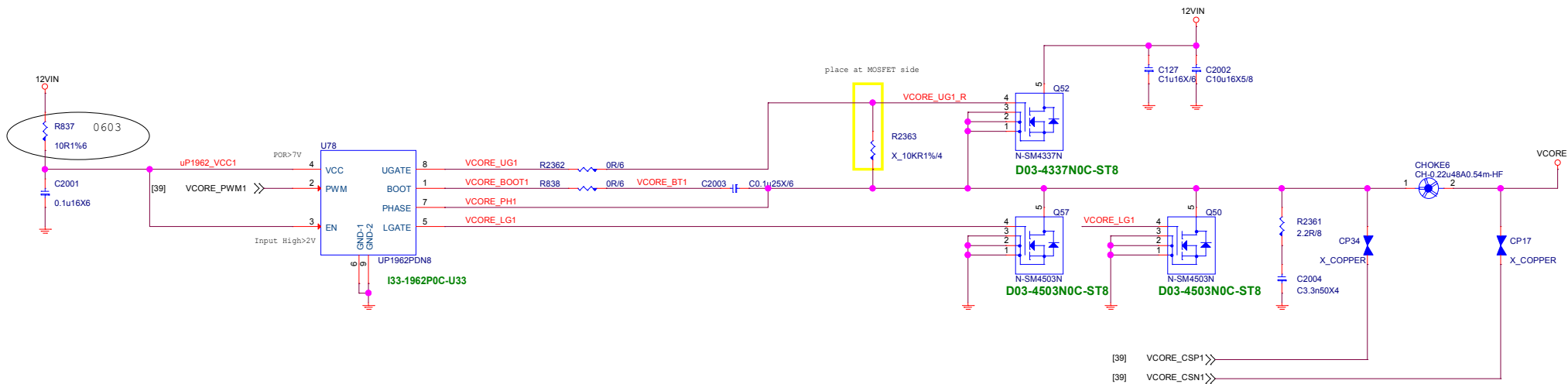
default:0.775V,0.2A



MP2143 has an open drain with 500kΩ pull-up resistor pin for power good (PG) indication.

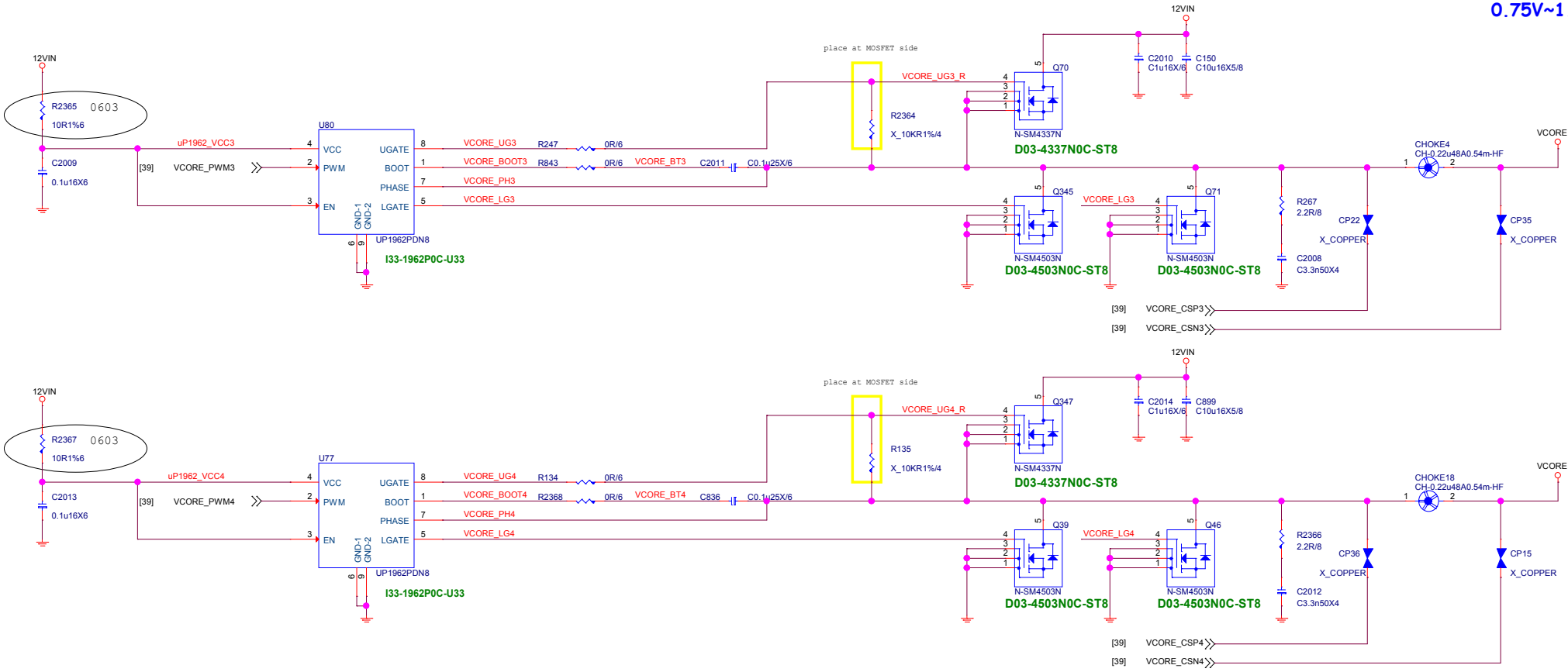
		BOOT VOLTAGE
SVC	SVD	Pre PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



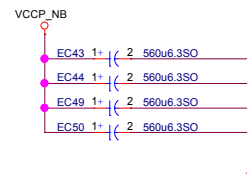
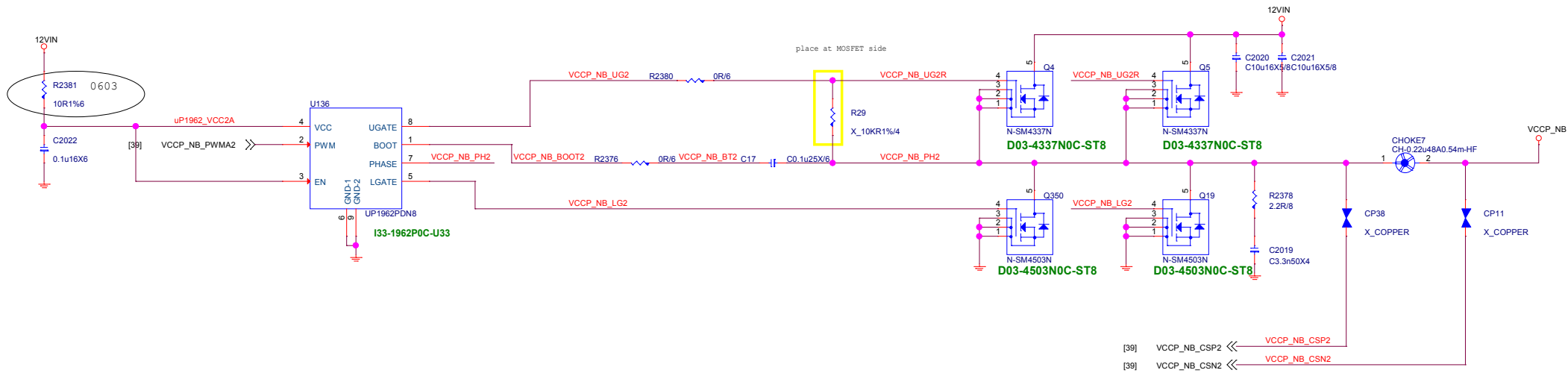
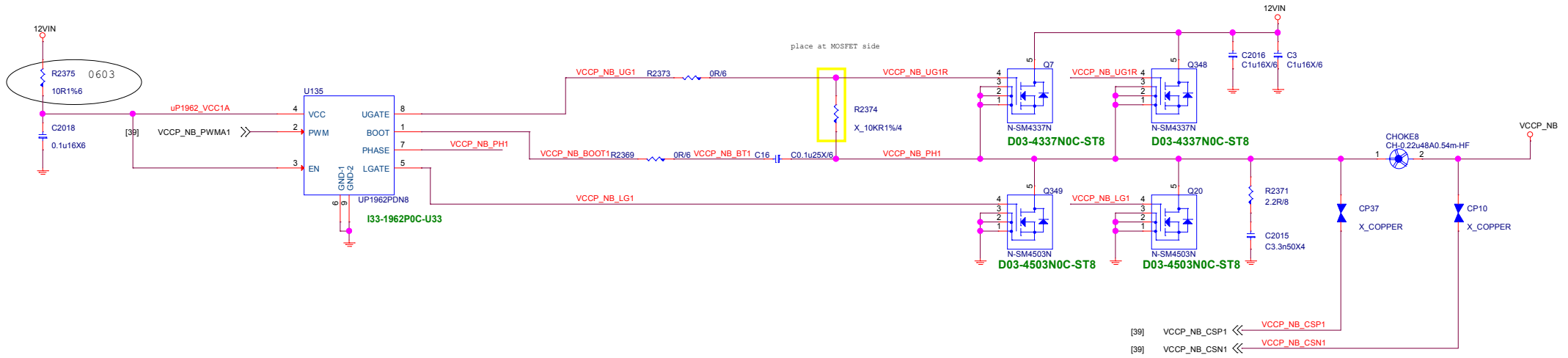


20170416

0.75V~1.2V



0.00625V~1.55V



FOR
VCCP_SOC_S5
0.9A

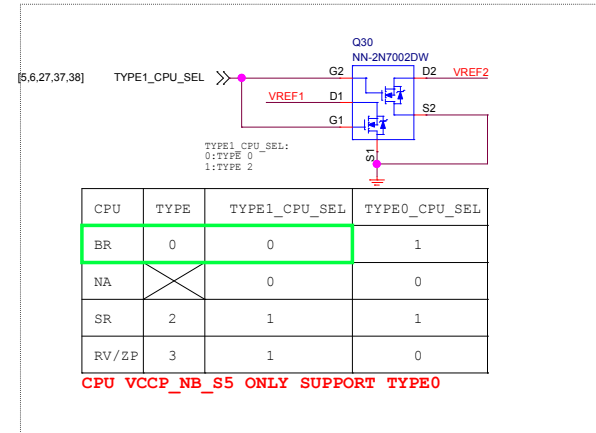
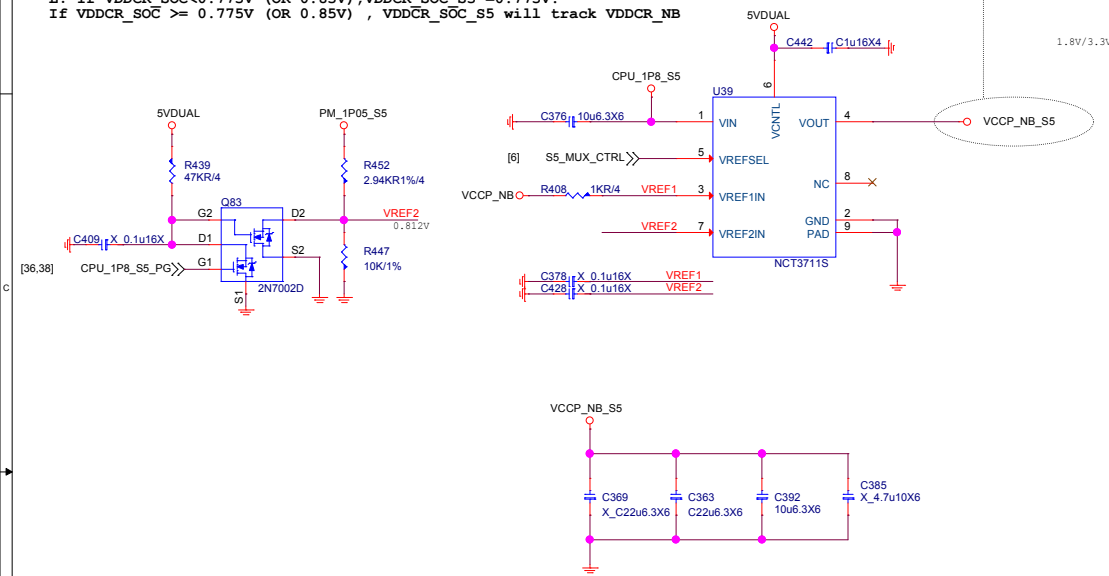
(VDDCR_SOC_S5 is only used for AMD TYPE0)

TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

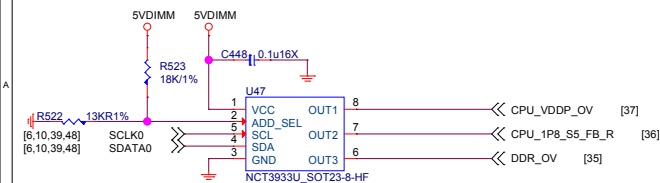
H: +VDDCR_FCH ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR SOC S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0

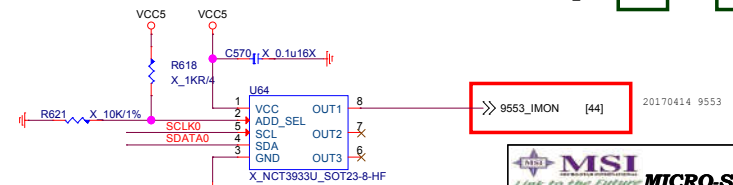


Over Voltage Control IC

0x26: RH=18K, RL=13K



0x2A: RH=OPEN, RL=10K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

MSI MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Switch / NCT3933 OV

Size: Custom

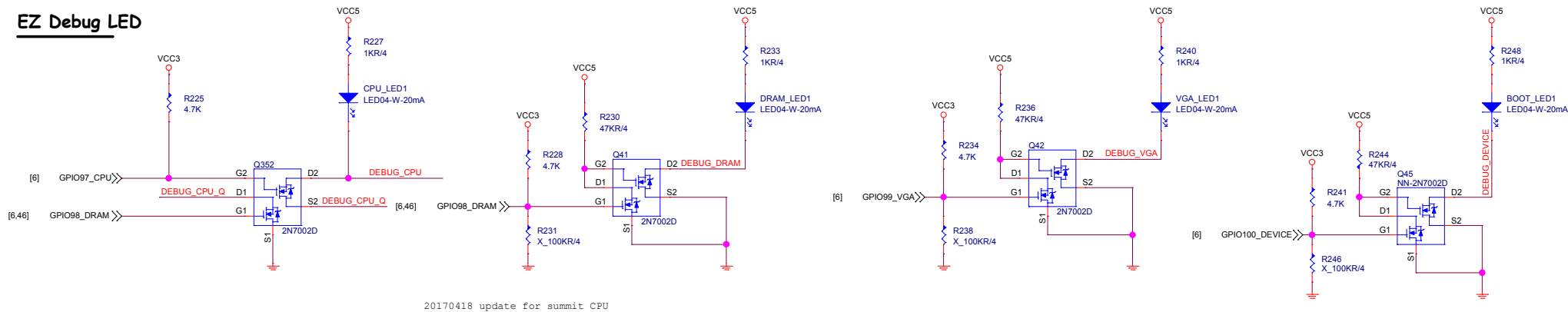
Document Number: MS-7B84..

Date: Monday, November 19, 2018

Sheet: 43 of 53

Rev: 20

EZ Debug LED

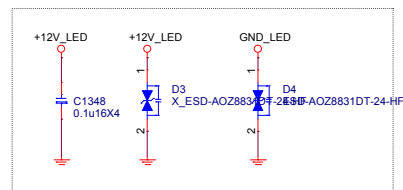
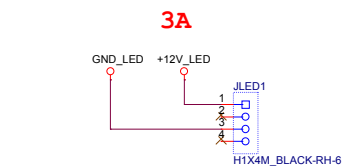
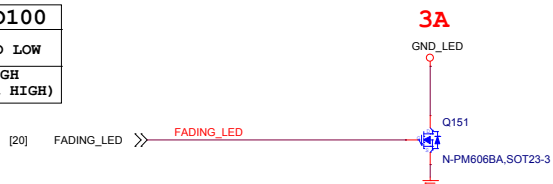
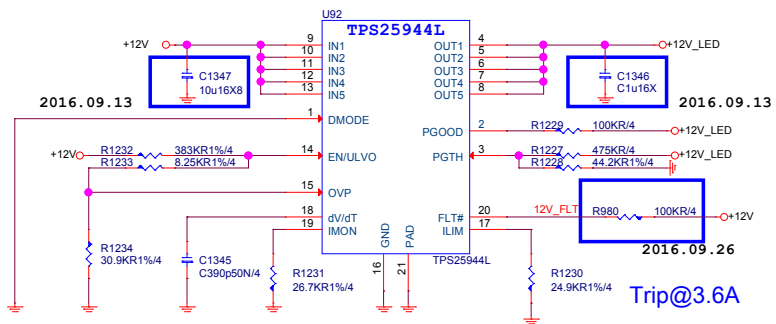


LED Control by SIO

JLED

2016.07.06 Use TPS25944L

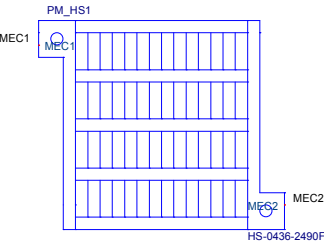
LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI FULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)



close to JLED1

AM4 APU Detect LED Circuit

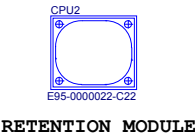
HEAT SINK



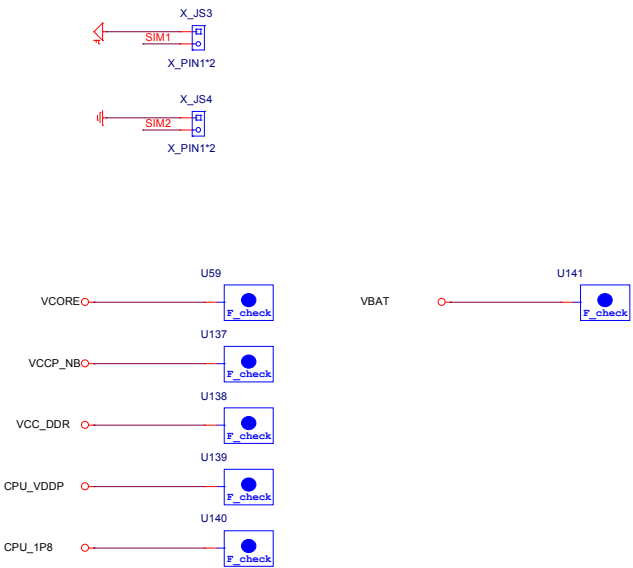
5010 Level



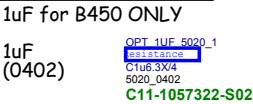
CPU Socket



Simulation



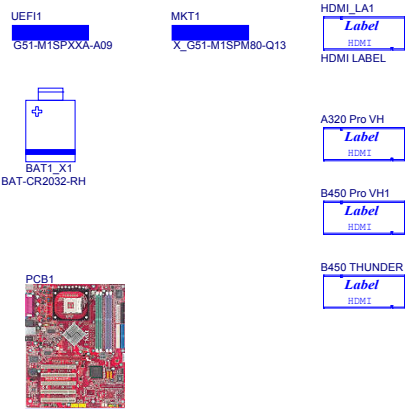
5020 Level



60 Level

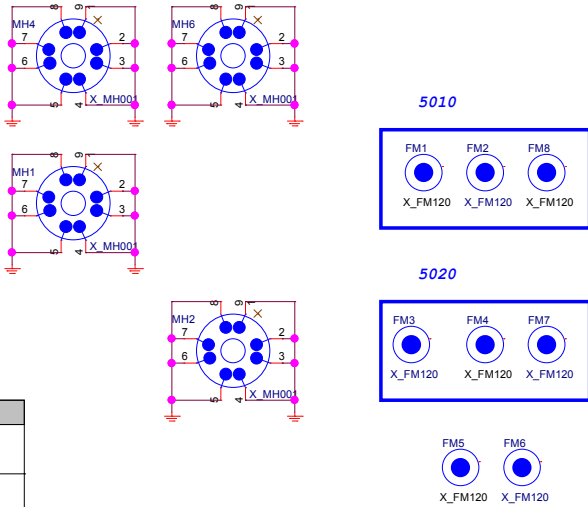
CAP USE N07 for A320/B450 SKU

MANUAL PART



PK0-07B8420-G37, 精成-深圳, 22, 寶安恩斯邁廠 (MSIS)
PK0-07B8420-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)

Optics Orientation Holes

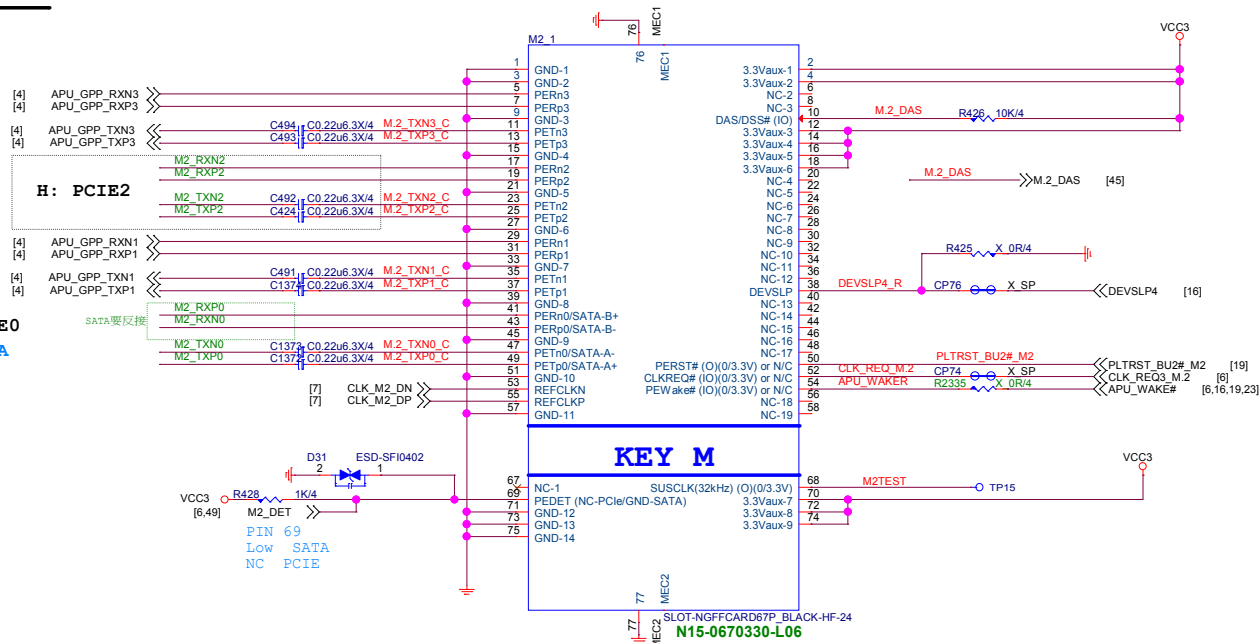


OPT	Configure	BOM	Function
		601-7B84-A01	XXXX

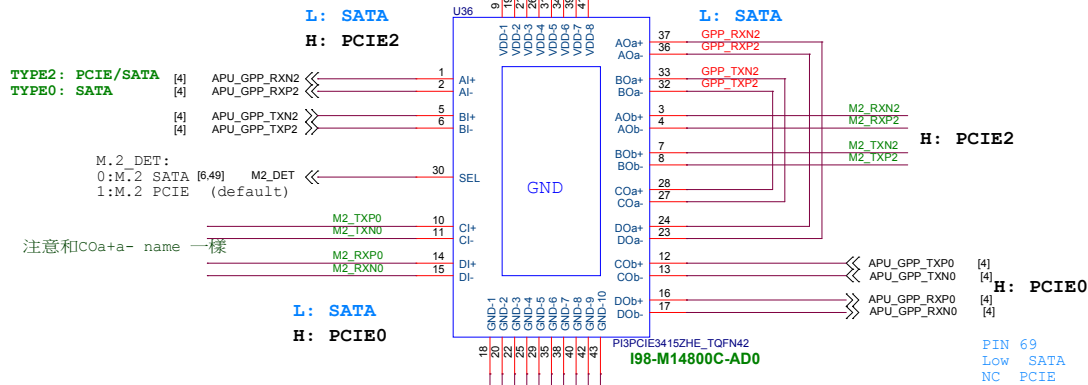
M.2 Connector

3.3V@2.5A

H: PCIE0
L: SATA



M.2 Switch



3.3V@2.5A

